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## DESIGN OF RADIATION HARDENED MNOS MEMORY

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SPERRY GYROSCOPE DIVISION  
GREAT NECK N.Y. 11020

SEPTEMBER 1975



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*This technical report has been reviewed and is approved for publication.*

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19. ABSTRACT (Continue on reverse side if necessary and identify by block number) This final report covers work performed in designing a CMOS/SOS memory subsystem based upon given specifications for a 256-bit memory chip. The subsystem interfaces with the Survivable MOS Array Computer (SMARC). Logic design and interconnection for the subsystem are presented herein. So too are the designs and specifications for the three chip types which satisfy all subsystem functions. In addition, the report presents estimates of the producibility and reliability for these chips for both conventional and hardened gate insulators.		

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## FOREWORD

This report was prepared by the Sperry Rand Corporation, Sperry Gyroscope Division, Great Neck, New York for the Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio. The work was performed under Air Force Contract No. F33615-73-C-1266, entitled "Design of a Radiation Hardened MNOS Memory", Project No. 3176, Task No. 3176-01-10, for the period June 1973 through June 1974, and administered under the direction of the Air Force Avionics Laboratory, Advanced Electronic Devices Branch. Dr. Ronald A. Belt (AFAL/TEA-3) was the Air Force Project Monitor.

Mr. John M. Rogers, Section Supervisor for Computer Devices, was Program Manager. Mr. Stephen G. Rogich was the Principal Investigator for this program. Other contributors to the program were: Dr. H. A. R. Wegener of the Sperry Rand Research Center, Mr. A. K. Rapp of Inselek Corp., and Mr. P. Marraffino of the Sperry Gyroscope Division.

This technical report was submitted by the author in December 1974.

Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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## SUMMARY

This report covers work performed in designing a hardened CMOS/SOS memory subsystem based upon given specifications for a 256-bit static EAROM memory chip. The subsystem is required to interface with the Survivable MOS Array Computer (SMARC). It is a program memory (on-line read only) with a basic size of 2048 36-bit words, expandable to 32,768 words. The specified read access and cycle times are 300 and 500 nanoseconds, respectively.

A logic design for the subsystem was generated; logic and interconnection drawings are presented in this report. The essence of the program is the design of the memory control chips which populate the subsystem. The design is such that only three chip types are required: 1) Chip type A, multi-function driver; 2) Chip type B, data output buffer; and 3) Chip type D, decoder, gates, and inverter. The total number of control chips is small, less than 12 percent of the number of memory chips. Chip design includes calculations of the size of all transistors and of the over-all chip, propagation delays and transition times, capacitance loading, and power dissipation. In addition, a sample layout drawing for two of the circuits used has been prepared.

The radiation hardening approach is specified and its effects upon performance, producibility, and reliability are discussed. The manufacturing cost increment for radiation hardened parts is estimated to be approximately 60 percent. The performance degradations comprise, essentially, increases in propagation delays of varying amounts, depending upon the degree of channel width compensation.

At the subsystem level, the total power dissipation is calculated to be about one watt for 2 megahertz operation. Standby power is less than 10 milliwatts for an 8K x 36 section of memory.

There is a discussion of packaging of the three control chips and the memory chips. The number of chips is large because of the small capacity of the memory chip and thus the SMARC circuit board approach is impractical. Instead, a ceramic hybrid package approach is suggested and its characteristics for other memory chip capacities are examined.

## Section 1

### PROGRAM OBJECTIVES

#### A. INTRODUCTION

This program was undertaken as a design effort for a memory subsystem which complements other Air Force programs involving the computer subsystem (SMARC, Survivable MOS Array Computer) and the memory devices themselves. The specific objectives were to evolve circuit designs and specifications, to determine the producibility of all memory subsystem devices (excluding the memory chips themselves) utilizing complementary metal-oxide-silicon circuits on a sapphire substrate (CMOS/SOS). In addition, the requirement that the devices be radiation hardened was imposed. In order to achieve a comparison, it was required that the circuit design be considered for both the conventional silicon dioxide ( $SiO_2$ ) gate insulator and a hardened gate insulator approach. The producibility, cost, and reliability of both approaches were to be established. In addition to the above requirements, which relate to the memory support devices per se, it was also required that over-all logic and interconnection drawings be generated that indicate how these devices are used with the memory devices to form the complete memory subsystem. Furthermore, packaging studies were called for which indicate how the devices, both memory and support, might be packaged in a manner compatible with SMARC system packaging concepts.

A summary of the objectives and tasks of this program is given in table 1. The objectives of the program have been accomplished in the manner presented in this final report.

Table 1  
OBJECTIVE

RADIATION HARDEDENED MEMORY SUBSYSTEM  
USING  
MNOS MEMORY DEVICES  
CMOS/SOS CONTROL DEVICES

TASKS

1. Logic and circuit design
2. Generate over-all logic and interconnection dwgs
3. Perform packaging studies
4. Generate functional specifications
5. Perform reliability studies\*
6. Make producibility evaluations\*
7. Generate cost estimates\*

-----  
\*For  $\text{SiO}_2$  and hardened insulators

B. MEMORY SUBSYSTEM REQUIREMENTS

The memory subsystem requirements are defined in the Statement of Work (SOW) and are summarized in table 2. Note that the memory is a program memory. Consequently, although the MNOS memory devices are inherently alterable, writing into memory is not part of normal on-line operation. Furthermore, it is not essential that the support circuitry to write into the memory devices be an integral physical part of the memory subsystem, although provision must be made for connections to external "write" circuitry. It turns out, however, that the inclusion of write and clear drivers for the memory devices is relatively inexpensive, requires no additional types of devices, and substantially reduces the number of connections that are required to external write/clear circuits. As a result, these drivers have been included in the memory subsystem design.

The basic configuration of the memory contains only 2048 words of 36 bits each. The maximum possible configuration, however, must be able to store 32K words (32,768).

Table 2  
SUBSYSTEM CHARACTERISTICS

DEVICES:

MNOS memory (program)  
CMOS/SOS control

SIZE:

Basic configuration = 2K x 36  
Expandable to 32K x 36 (1K increments)

SYSTEM:

Survivable MOS array computer (SMARC)

SPEED:

Read access = 300 ns  
Read cycle = 500 ns

POWER:

5 watts maximum, 1 watt goal (for 2K x 36)  
+10V, +20V, -20V

PACKAGING:

Flat packs on wire-weld boards  
One 8.6" x 9.0" board per 8K x 36

In all cases, 32 bits of the word contain program data and the remaining four bits are used for parity checking. No parity generation nor checking circuits are required in the memory subsystem.

It should be noted that the original intent was to house one-quarter of the full capacity (i.e., 8K (8192) words) on a single board, also known as one "section" of memory. A full system would thus comprise four boards. Each section, or board, is required to stand on its own, i.e., to contain complete interface circuitry for address decoding, data buffering, control logic, etc. Although the memory chip size (256 bits)

makes the mounting of an 8K x 36 memory subsystem on a single board virtually impossible, the design has been carried through as four 8K x 36 sections. The matter of packaging alternatives is discussed further on in this report.

A block diagram of the major parts of one section of memory is given in figure 1. It indicates that the basic memory consists of 2048 words (two 1K x 36 blocks) and that the expandability is in additional increments of 1K x 36 blocks of memory devices and additional address and chip select drivers to control those blocks.

The Mode Control block receives a pair of coded access mode signals from the computer which define the operation to be performed as follows:

ACCESS MODE SIGNALS

<u>A</u>	<u>B</u>	<u>OPERATION</u>
0	0	Read designated address
0	1	Clear designated address (to zero)
1	1	Alter designated address (to input data)
1	0	Not allowed; Access Error

If the last combination (1, 0) of signals occurs, logic must detect the condition and send an Access Error signal to the computer. This logic must exist independently in each section of the memory. However, there is a case under which this condition should not result in an Access Error to the computer, the case in which the address designated by the address lines from the computer refers to a nonexistent memory location. For example, in a system that employs only 16K words of memory, any address between 16K and 32K would be invalid. The memory subsystem would be required to recognize this condition, generate an Address Error, and suppress an Access Error (if the invalid access mode combination exists).

The Memory Timing block receives timing signals from the computer and directs operations accordingly. The timing signals are shown in figures 2, 3, and 4 for read, clear, and alter cycles, respectively. The period, T, is specified in the Statement of Work to be either 320 nanoseconds or 480 nanoseconds. However, although the computer is able to provide either period, so that memories of different speeds might be employed, it was not established during the course of the contract that the 256-bit memory device would, in fact, permit operation at even the slower cycle time.

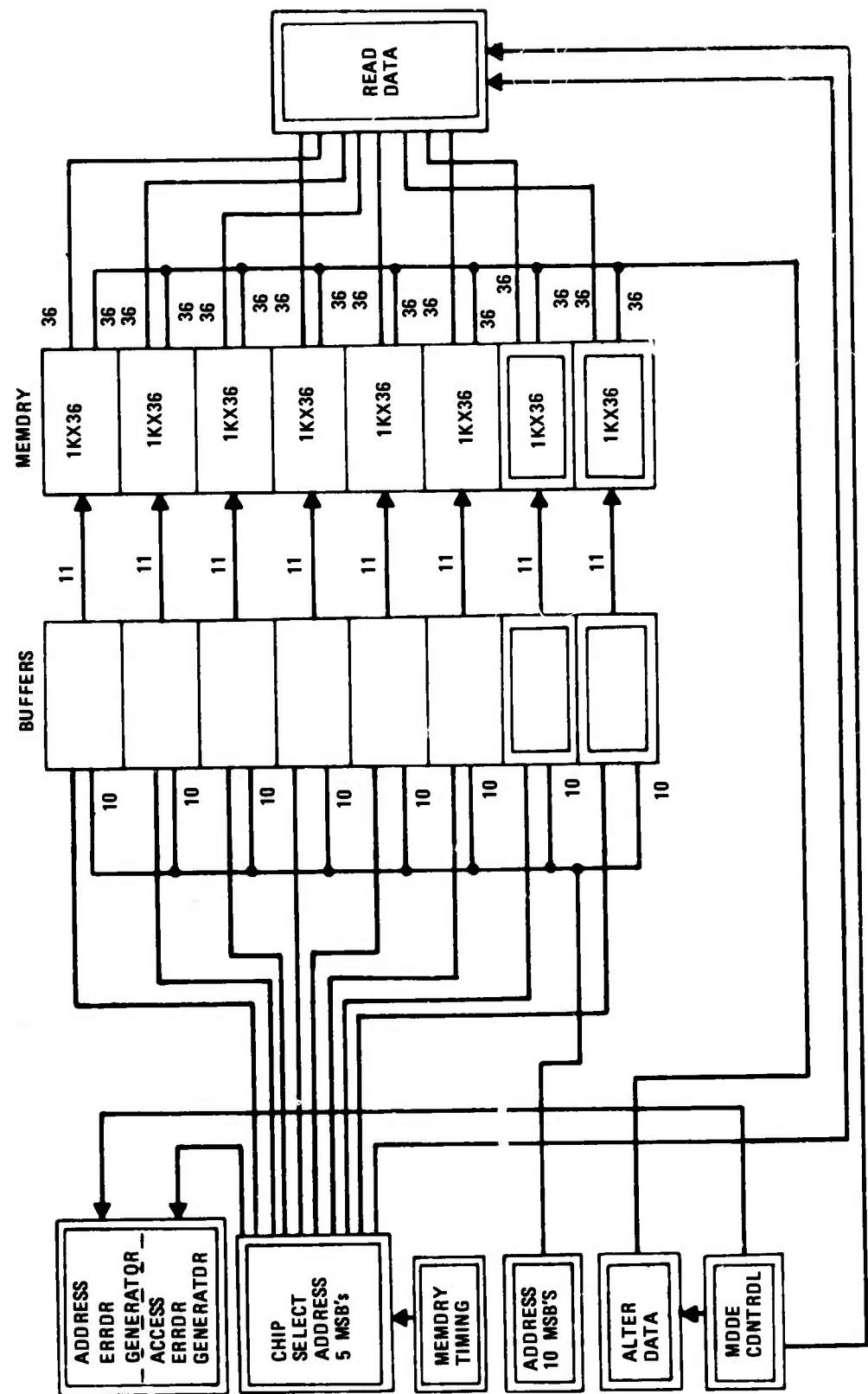


Figure 1. MNOS ROM Section (8K x 36)

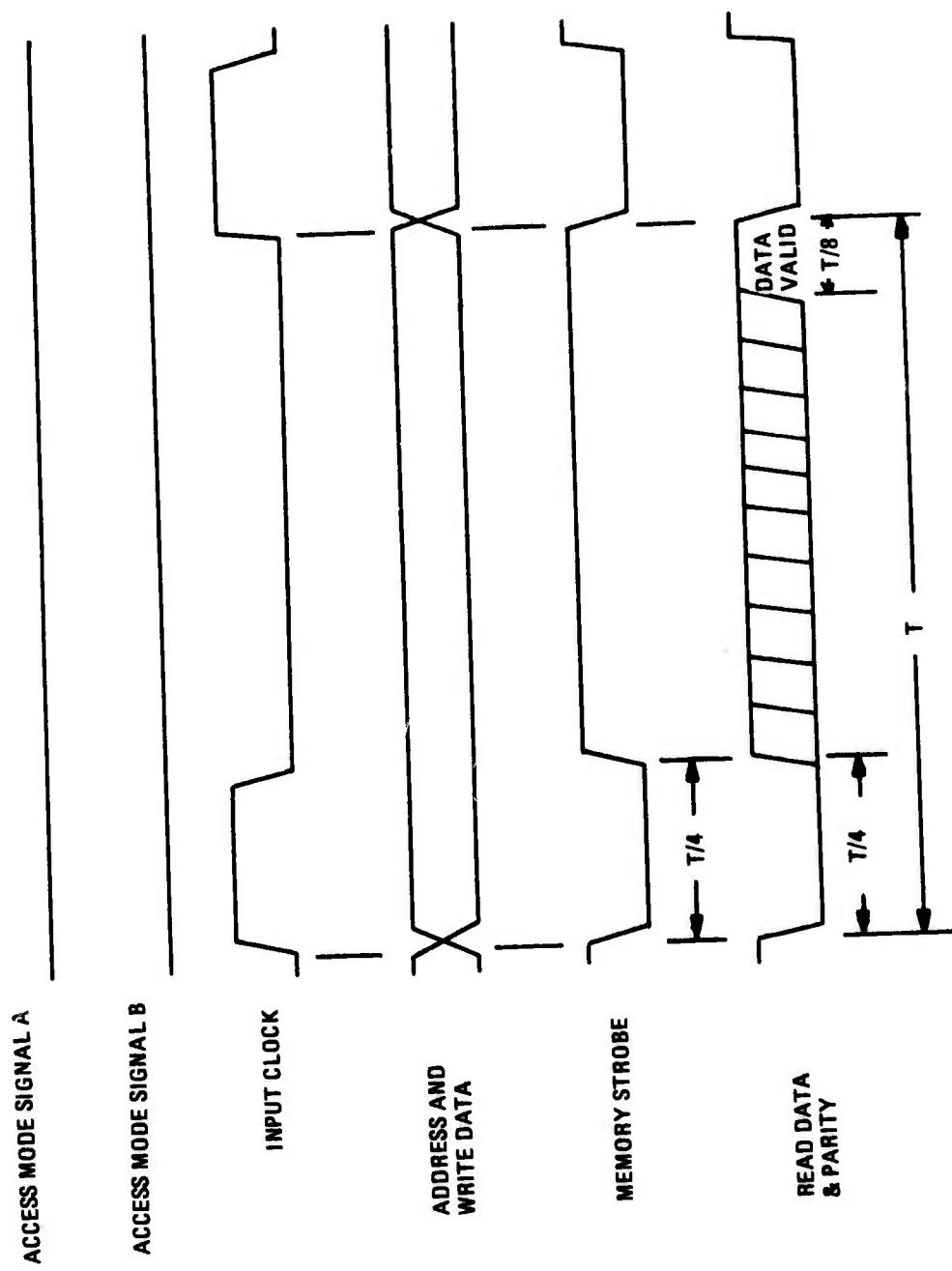


Figure 2. Memory Read Timing

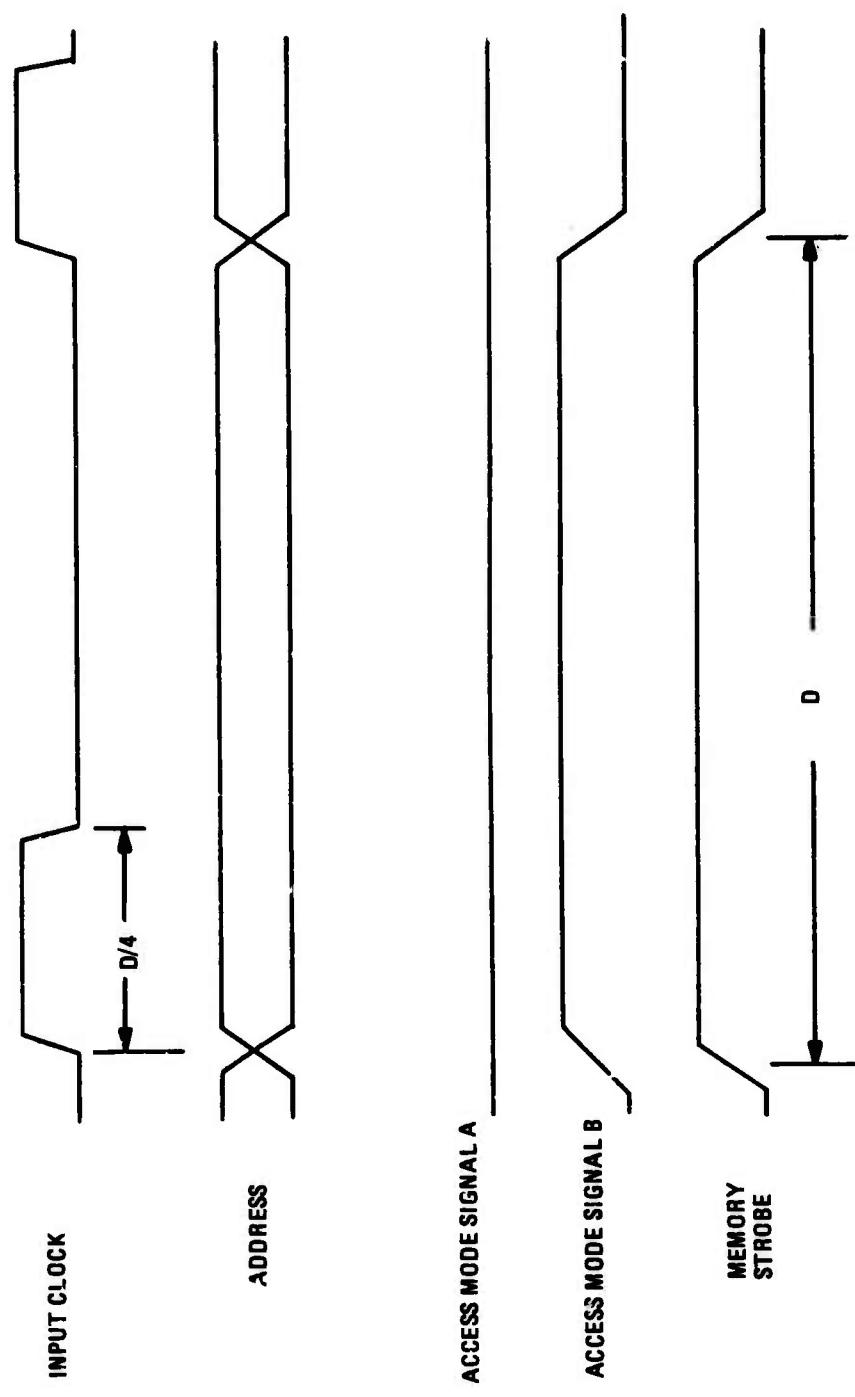


Figure 3. Memory Clear Timing

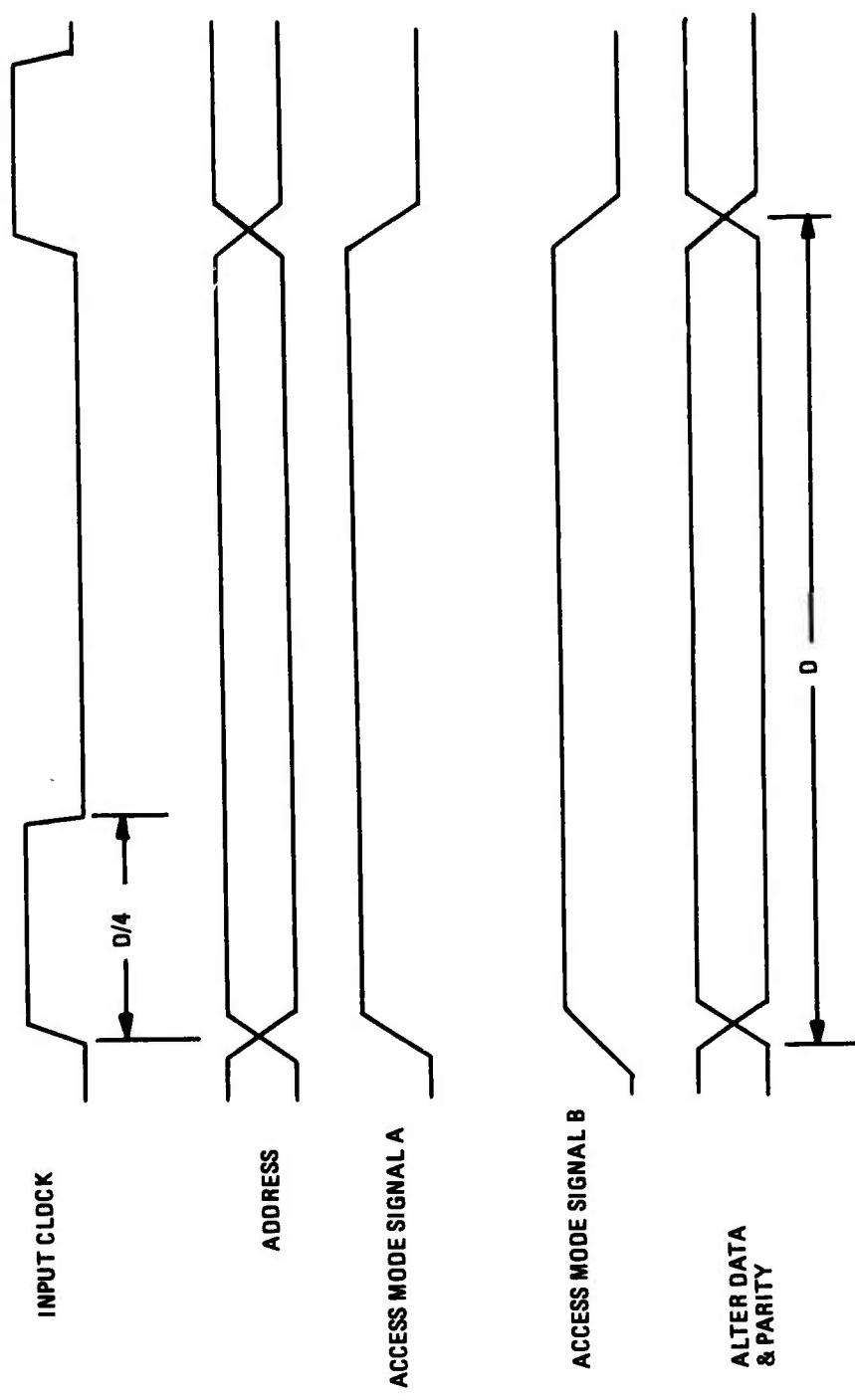


Figure 4. Memory Alter Timing

The approach taken, therefore, was to endeavor to make the support chips as fast as possible so that they would not contribute excessively to the over-all access and cycle times. The values achieved are shown in Section 2 of this report. The duration, D, indicated in figures 3 and 4 is the minimum time required to satisfy the retention specification of  $10^4$  hours. The SOW requires that D be less than 1 millisecond.

### C. INTERFACE TO COMPUTER SUBSYSTEM

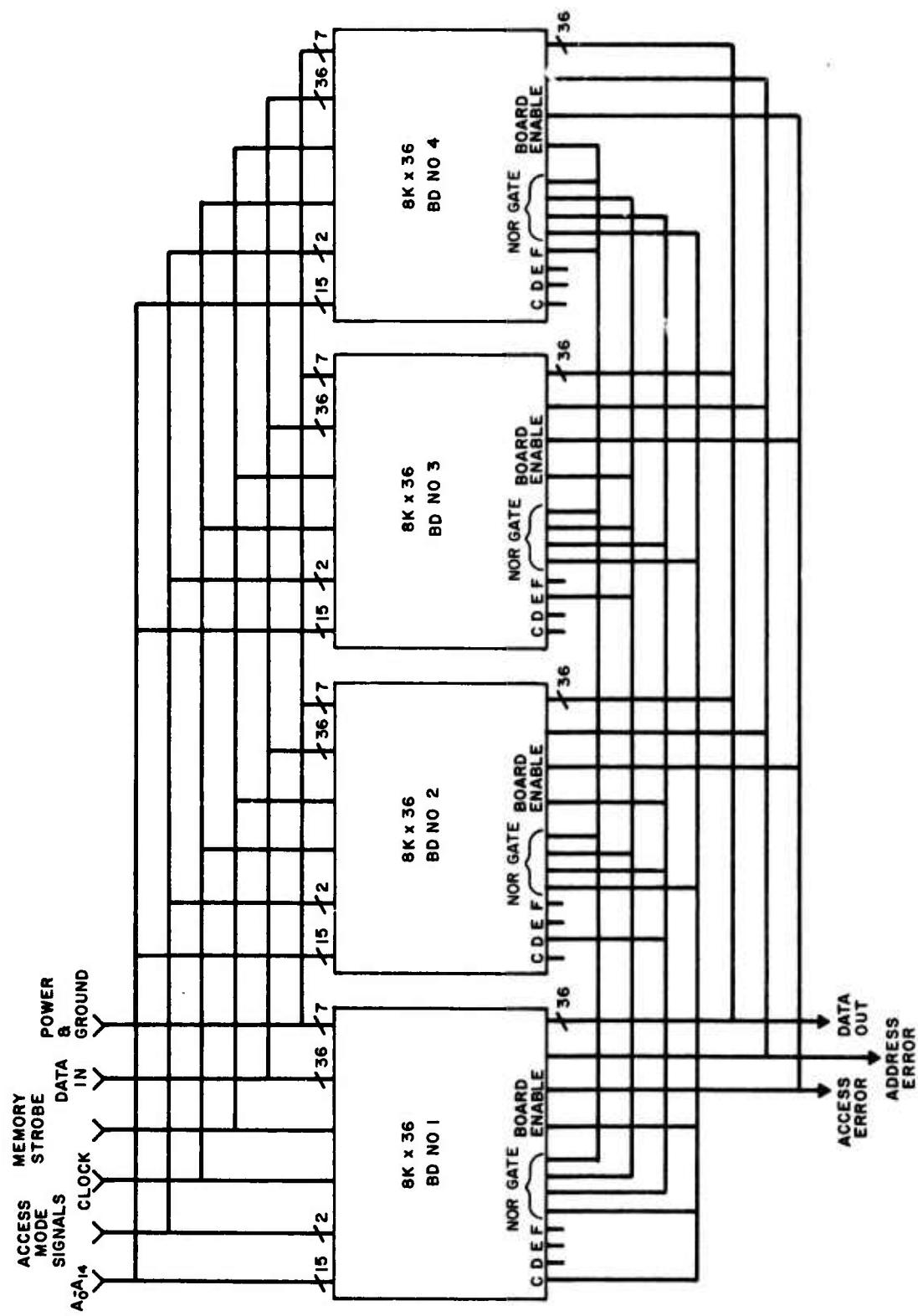
The interconnection of four 8K x 36 sections to form the full configuration memory is shown in figure 5. In addition, this diagram also shows all of the 100 interconnections to the computer subsystem specified in the SOW. There are 62 input lines as follows:

1. 36 data inputs (including the four parity bits)
2. 15 address lines
3. Access mode signals A and B
4. Clock
5. Memory strobe
6. +10 volts, +20 volts, -20 volts and four ground wires

There are 38 output lines consisting of the 36 data outputs (including the four parity bits), Access Error, and Address Error. It should be noted that the voltages supplied do not fully meet the supply voltage requirements of the memory chip (See subsection 1D).

All of the interface signals have the following electrical characteristics:

1) Logic "1" is an open circuit voltage of  $+10.0 \pm 0.5$  volts dc with an output resistance of less than 1000 ohms and 2) Logic "0" is an open circuit voltage of  $0.2 \pm 0.2$  volts dc also with an output resistance of less than 1000 ohms. No specification on capacitive loading was given, a discussion of which is included in Section 3 of this report. The SOW required that the transition times of outputs from the memory to the computer be  $25 \pm 5$  nanoseconds. This has been implemented in the chip designs using an estimated capacitive loading of the computer circuits.



#### D. MEMORY DEVICE CHARACTERISTICS

At the outset of this program, there were two memory devices intended to be used as the basis for memory subsystem design. It was desired to achieve the capability to use the control devices with one memory device in some applications and with the other memory device in different applications. Neither device existed as a final design with firm specifications, however, and unfortunately that situation persisted throughout this contract.

One device is being developed by General Electric under contract F33615-72-C-1706. It was initially intended to be a 2048-bit chip but the design has since been modified to a 1024-bit chip. The other device is being developed by RCA under contract F33615-72-C-1679. It was originally planned to be a 1024-bit chip but the requirements have since been modified to specify a 256-bit chip. The originally-specified characteristics of the two chips and the characteristics of the smaller RCA chip are shown in table 3. The characteristics of the smaller GE chip were not received during this program.

It became apparent after additional memory chip information was received during the program that a subsystem design able to accommodate both devices was not feasible. In addition to the increased disparity in the storage capacity of the two devices, the following significant differences were found (see table 4): 1) the GE memory is dynamic and requires several clocking signals which the static RCA device does not; 2) the GE chip requires several signals that are greater than 10 volts in amplitude, whereas the RCA device is fully compatible with a CMOS interface that uses 10-volt swings; and 3) the GE chip has data input and output on the same pins, whereas the RCA chip has separate sets.

Memory chip specifications required for a design of the support chips were not available for the RCA chip until considerably later than those of the GE chip. Consequently, the interim report on this contract (Sperry report no. SGD-4282-0738, March 1, 1974) considered memory driver design in terms of the GE memory chip. Since that time, the RCA device information became available and the decision was made to use it as the basis for the memory subsystem design.

Table 3  
MEMORY CHIP CHARACTERISTICS

SPECIFICATION	2048 CHIP	1024 CHIP	256 CHIP
1. Organization	512 x 4	256 x 4	64 x 4
2. Decoder	MNOS	CMOS/SOS	PMOS/SOS
3. Variable threshold $V_G$	30V max	30V max	30V max
4. Decoder threshold V	1V max	TTL compat.	TTL compat.
5. Thin $SiO_2$ thickness	30 Å max	30 Å max	30 Å max
6. Avg. power dissipation	500 mW max	500 mW max	500 mW max
7. Read cycle	500 ns max	200 ns max	600 ns max
8. Write cycle	1 ms max	1 ms max	1 ms max
9. Operating temp. range	-55° to 125°C	-55° to 125°C	-55° to 125°C
10. Radiation hardness	$10^6$ rads min	secret	secret
11. Environmental	MIL-STD-750A	MIL-STD-883A	MIL-STD-883A
12. Retention time	24K hrs min	25K hrs min	25K hrs min

Table 4  
MEMORY CHIP DIFFERENCES

SPECIFICATION	2048 CHIP	256 CHIP
1. Organization	512 x 4	64 x 4
2. Peripheral circuits	Dynamic	Static
3. Data I/O pins	Common	Separate
4. Total pins	25	22
5. Read control signals	6	None
6. Signal swings	0 to 10V 0 to 20V	0 to 10V

The reasons for choosing the RCA device were: 1) its full CMOS compatibility; 2) its ease of use deriving from the employment of static memory cells; 3) the expected radiation resistance benefits of the static design and SOS technology; 4) the compatibility of its separate data input and output pins with the SMARC computer system interface; and 5) the existence of potential back-up sources for a 256-bit device.

A block diagram of the RCA memory chip is given in figure 6. Table 5 lists the performance characteristics and supply voltage requirements and figure 7 shows operating waveforms.

Although the information concerning the RCA memory chip was acknowledged to be tentative, pending characterization of prototype units, it was used, of necessity, as the basis for memory support chip design. In addition, an input capacitance of 5 picofarads on all inputs was postulated, based upon the information that the chip design includes buffered inputs to minimize loading.

Two particular difficulties involving the memory chip characteristics should be noted relative to the subsystem requirements imposed by the Statement of Work.

One is the discrepancy in signal voltage swing: the memory chip swings are specified to be from ground to -10 volts, whereas the SOW requires interface swings between ground and +10 volts. The second is the power supply levels required by the memory chip, voltages which are not available from the system according to the SOW.

One can probably solve the first problem simply by increasing all of the chip power supply voltages by 10 volts to:  $V_{DD} = GRD$ ,  $V_T = +7.5V$ ,  $V_W = -15V$ ,  $V_R = +5V$ , and  $V_{SS} = +10V$ . The discrepancy of these supply voltages, except for  $V_{SS}$ , with the voltages supplied by the system (+10V, +20V, and -20V) still remains. It is not within the scope of this contract to resolve this problem. In addition, the memory chip information is tentative and may yet change.

Table 5  
MEMORY CHIP SPECIFICATIONS

Supply voltages:	$-V_{DD} = -10$ volts
	$-V_W = -25$ volts
	$-V_R = -5$ volts
	$-V_T = -2.5$ volts
MNOS threshold voltages: (At 50 $\mu$ A S-D current)	"0" state = -4 volts "1" state = -1 volt
Data output loading (max.):	15 pf
Timing specifications (approx.)	
$t_{CL}$	50 ns
$t_{CW}$	25 ns
$t_{R/W}$	60 ns
$t_{Din}$	20 ns
$t_{CP}$ , $t_{WP}$	depend upon write characteristics of MNOS memory devices

Values are for ambient temperature of 300°K

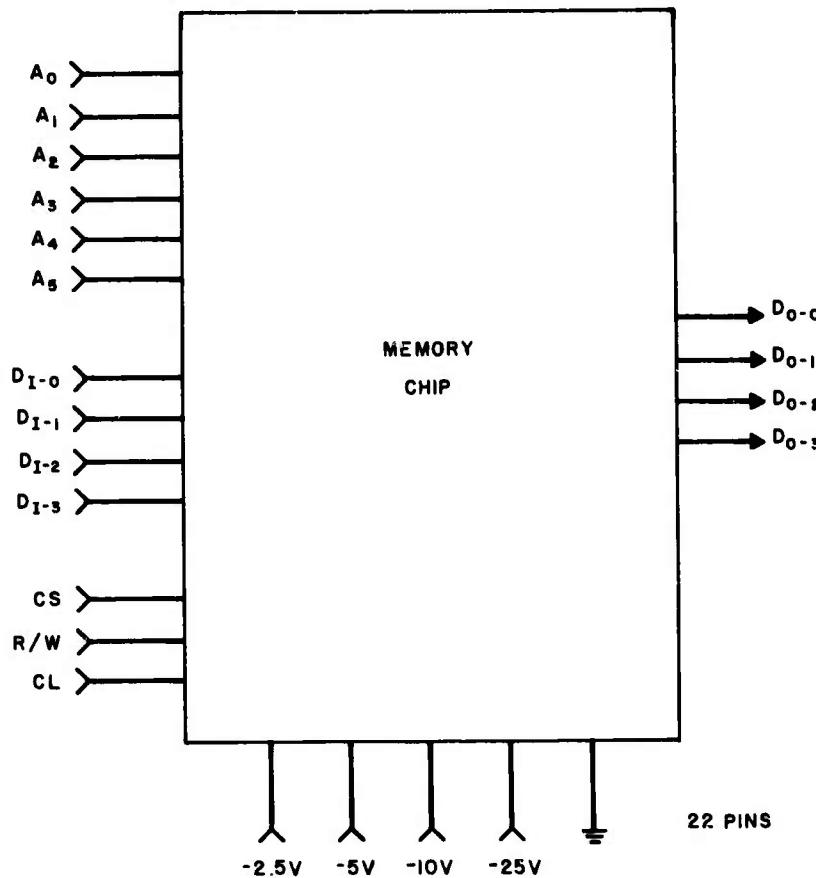


Figure 6. 64 x 64 MNOS Memory Chip

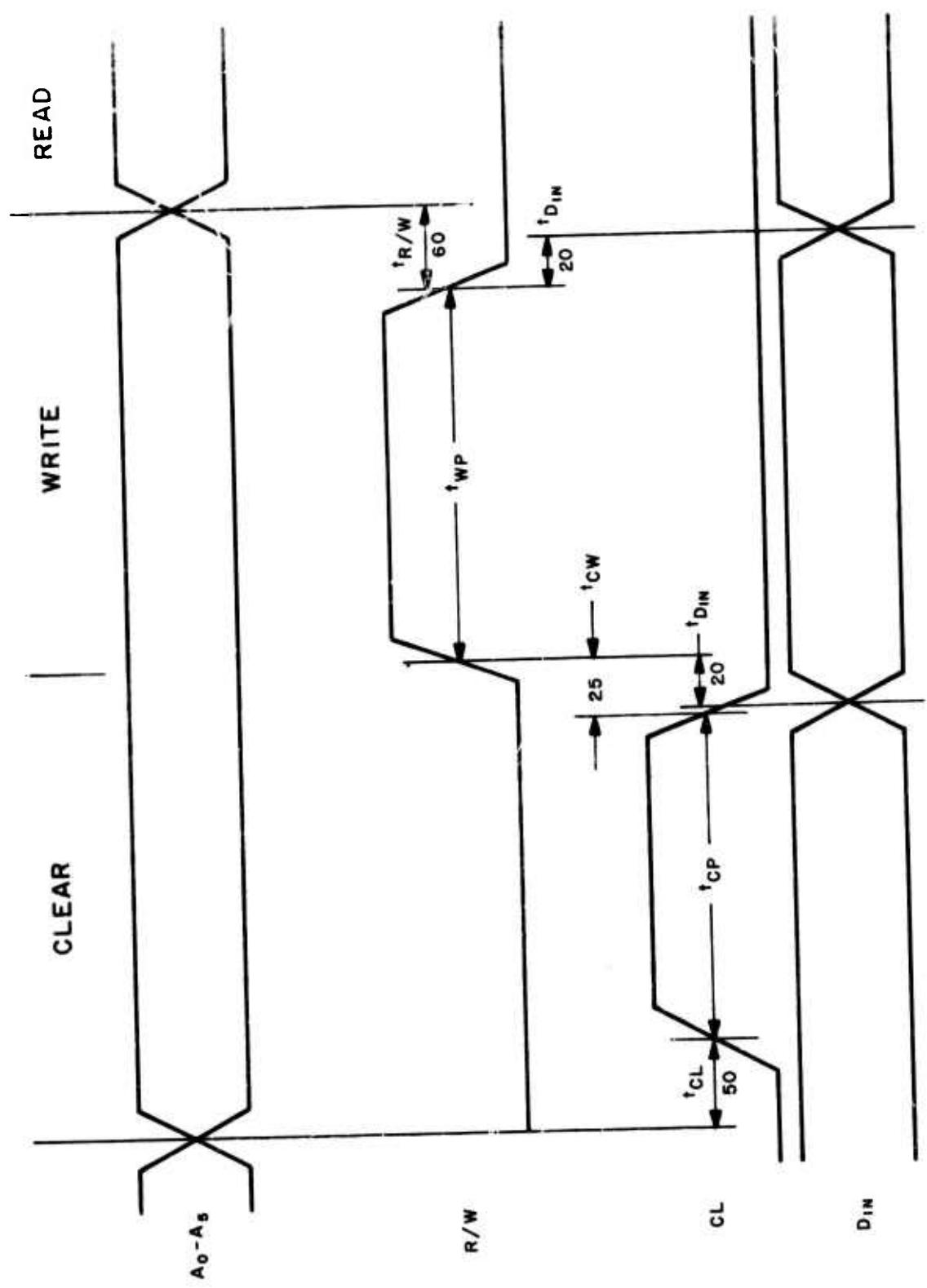


Figure 7. Memory Chip Waveforms

## Section 2

### SUBSYSTEM CIRCUIT DESIGN

#### A. INTRODUCTION

In general, one designs the logic of any given system with a predetermined family of logic elements in mind, although one may design generally and make a later adaptation to the chosen family of circuits. In the course of this program the approach taken was actually a combination of these two methods. The nature of this contract calls for custom circuits, primarily because of the radiation-hardening requirement. There currently exists no family of suitable CMOS/SOS elements that might serve as the basis for subsystem design. The nature of the memory subsystem is such that the bulk of the circuits required are drivers for the various memory chip inputs and output buffers for the memory chip outputs. There are relatively few circuits needed for logic, per se. The differing natures of drivers, output buffers, and miscellaneous logic render it impossible to use the same circuit type for more than one of these three areas. Consequently, it is highly desirable to have only three circuit types, one for each of these applications, to minimize development and production costs, and to simplify spare parts logistics. Such has, in fact, been achieved on this program. The three chip types which have been designed are:

- Chip type A: multi-function driver
- Chip type B: data output buffer
- Chip type D: decoder, inverter, and gates.

To answer the question that immediately pops to mind: there was a type C chip at one point in the program but it was superseded and the designation D (standing for "decoder") was given to the later chip type.

The type A and B chips were designed on the bases of the quantities and loading and drive characteristics of the memory chips. The memory subsystem was then designed using general NAND/NOR gates, inverters, and decoders. After that came the conception of a single chip type (type D), capable of satisfying all circuit needs beyond those of the type A and B chips. The memory subsystem was then laid out specifically in terms of the type A, B, and D chip elements. For example, the initial logic design included 3- and 4-input gates in some instances. In the final design, only the 2-input gates of the D chip are employed. This is because the threshold voltage changes in a radiation environment produce shifts in voltage transfer curves which are more accentuated in 3-input gates and even further aggravated in 4-input gates.

The evolution of the three chip types and their characteristics are presented in the following three sections of this report. Their interconnection as a subsystem is presented later, in Section 3, for the sake of increased clarity and understanding.

#### B. CHIP TYPE A: MULTI-FUNCTION DRIVER

One of the principal objectives in the design of the driver was to satisfy the driving requirements for all inputs to the memory chip so that only one chip type was required. This was facilitated by the fact that all memory chip inputs require the same voltage swing (10 volts) and are also buffered on-chip so that they present a low input capacitance (approximately 5 picofarads).

The first determination which had to be made was the desired number of drivers in a single chip. The resolution of this question can be appreciated best by reference to figure 8. The array of memory chips for a single section of memory (8K x 36) consists of 128 rows (128 x 64 words/chip = 8K words) and nine columns (9 x 4 bits/chip = 36 bits).

Consider first the address lines. From a functional standpoint, each address line is common with the corresponding address lines of every other memory chip in the entire array. However, if there were such a physical connection it would present a huge capacitive load of almost 6000 picofarads (1152 chips x 5 pf/chip). Furthermore, the power involved in charging such a huge capacitance would be largely wasted because only the selected row of nine chips is read out or written into at any given time. Consequently one must allocate some number of rows as the optimum load for a driver. In addition,

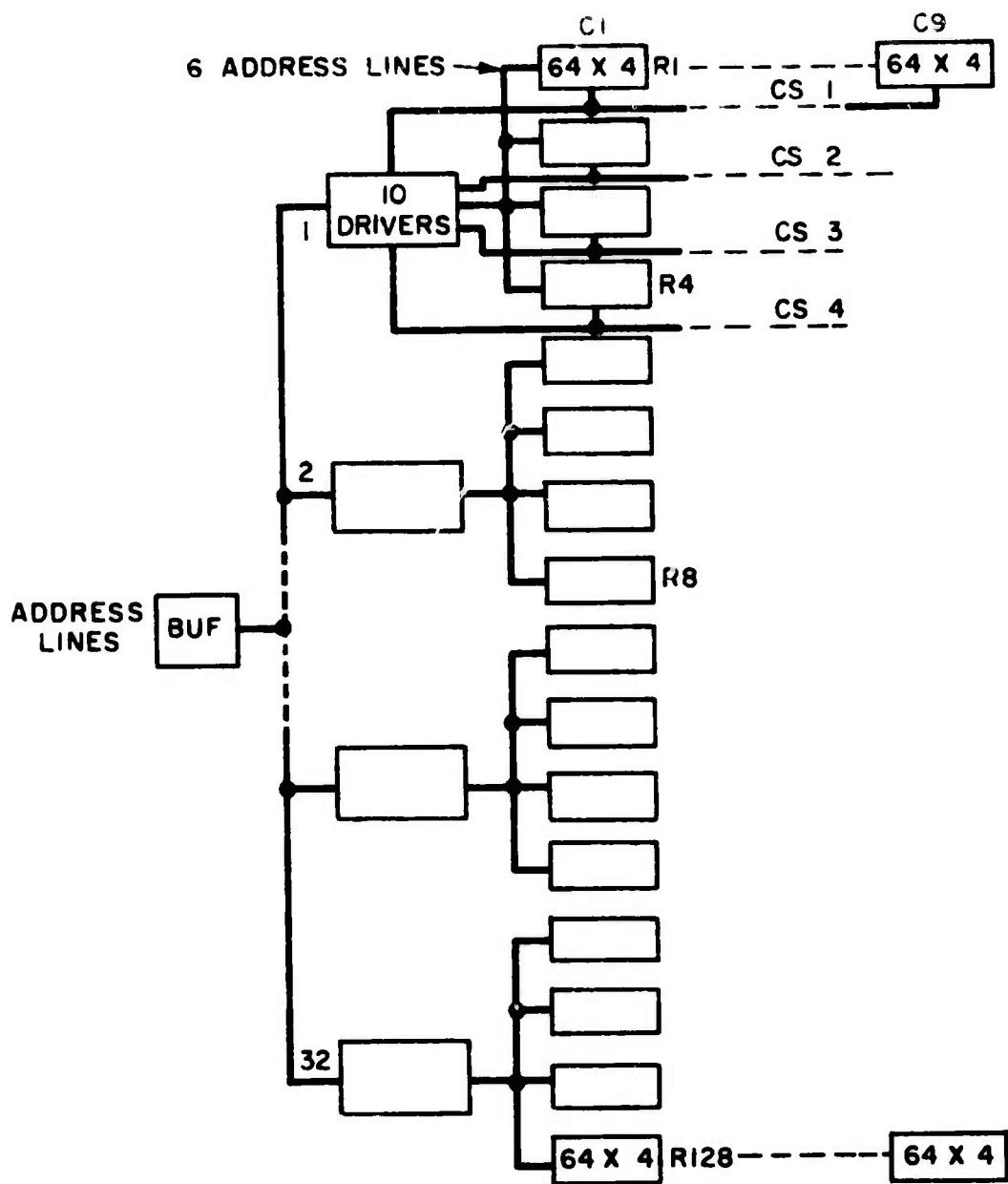


Figure 8. 128R x 9C Array

this number should be binary so that an exact division of the 128 rows of chips is achieved. A single row of memory chips represents a load of 45 picofarads for each of the six address line buses (9 chips x 5 pf/chip). Two rows represent a load of 90 pf, four rows gives 180 pf, eight rows give 360 pf, and so on. Calculations established that a 10-driver chip in which each circuit can drive 360 pf while presenting only 5 pf input capacitance entails a chip size that is beyond the present and near-term future state of the art. Ten circuits able to drive 180 pf, each, on the other hand, are producible at today's state of the art. Descending to the next level of 90 pf loading results in twice as many driver chips and heavier loading on the circuits which must drive the drivers themselves. These trade-off considerations strongly suggest designing for a load of 180 pf. When one makes the additional consideration of also using such a design for the data input drivers, the same advantages accrue. In this case, only nine of the 10 drivers on a chip are required because four blocks of nine satisfy the 36-bit word length. The leftover drivers can be used in many cases as will be shown in Section 3. This is because the chip (figure 9) is designed with two separate ENABLE lines, one controlling nine drivers, and the other a single driver. When using the chip to drive address and chip select lines both ENABLE lines are tied together. Figure 10 shows the correlation of logic symbols used for chip definition and schematic diagrams.

Note that each driver circuit contains four inverting stages in series. This produces a noninverting operation which is considered advantageous for flexibility. In addition, the use of four stages, rather than the three that would have been employed to obtain an inverting circuit, permits incorporation of additional capacitance gain so that the input capacitance to the driver can be reduced below the design goal of 5 pf to 3.4 pf. This is true of all 10 driver inputs and also of the ENABLE No. 2 input. It is not true of the ENABLE No. 1 input, whose input capacitance is 10 pf. The reason for this exception is that the inverter which is connected to this input "sees" a capacitive load that is nine times as large as the inverters connected to the other eleven inputs. It is possible to make this inverter of sufficiently small geometry to reduce the input capacitance to 3.4 pf. The penalty which would have to be paid is a propagation delay increase of about 18 nanoseconds. This was deemed excessive, especially considering that the propagation delay through the ENABLE No. 1 path is already about 6 nanoseconds larger than the other delays. Furthermore, a review of the subsystem interconnections revealed that the largest number of ENABLE No. 1 inputs that must be driven by a single

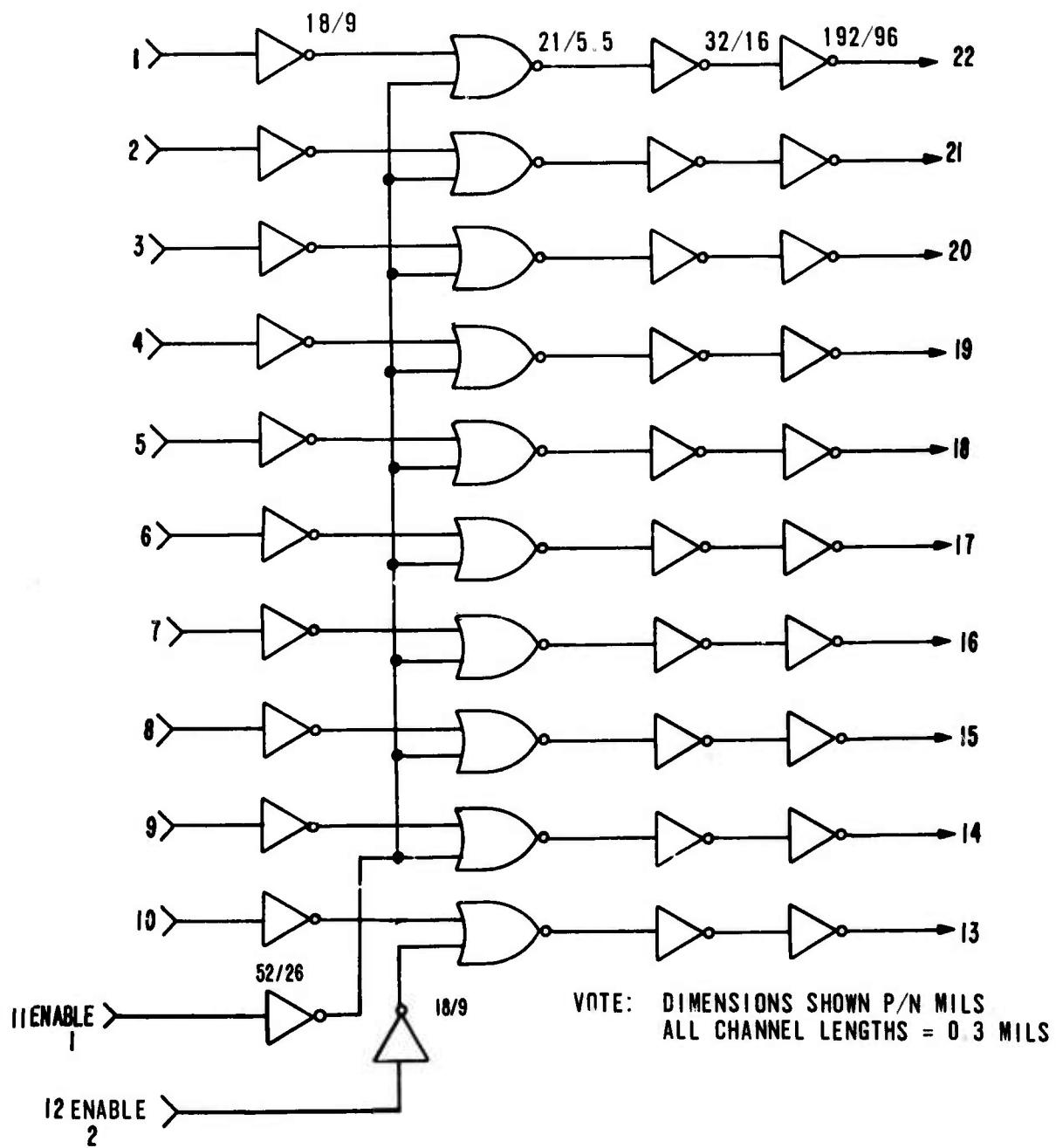
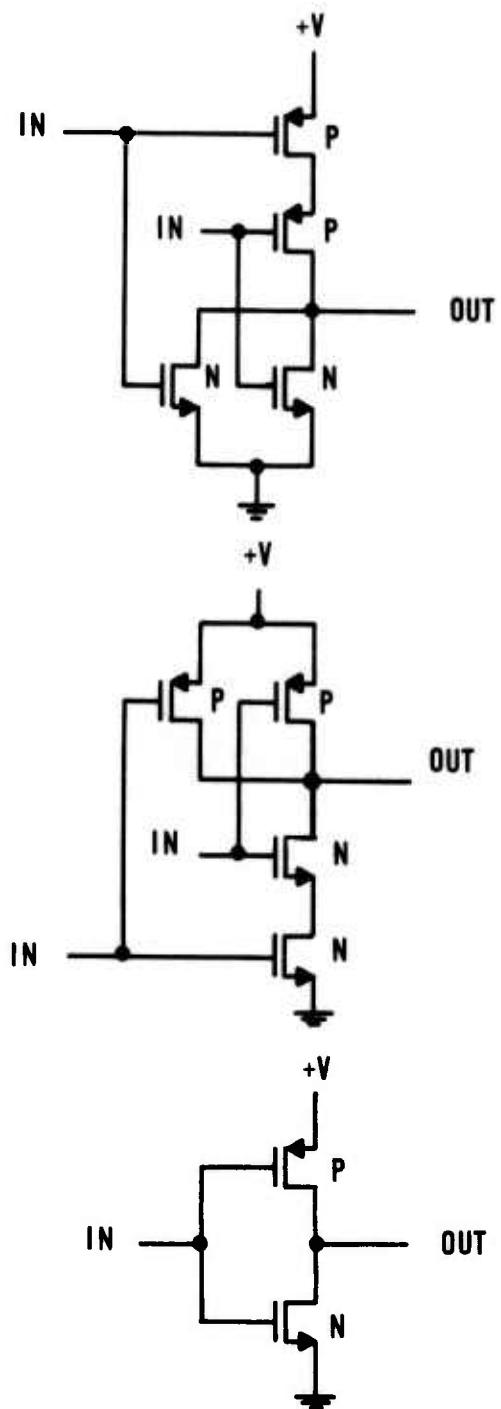
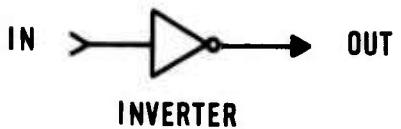
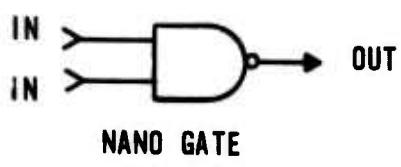
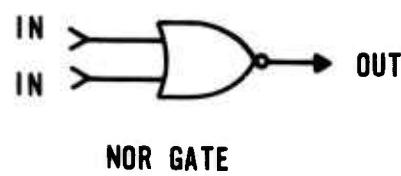


Figure 9. Multi-Function Driver, Chip Type A



**Figure 10. CMOS Logic/Schematic Equivalence**

node is five (decoder D1, pins 19-22 in figure 16). This adds up to 50 pf, which is the design load for the decoder outputs.

The characteristics of the Type A chip are summarized in table 6.

Table 6

CHIP TYPE A: MULTI-FUNCTION DRIVER CHIP

Number of drivers	10
Number of ENABLE lines (active high)	2
Chip size	145 x 145 mils
Input capacitance	
Driver inputs and ENABLE No. 2	3.4 pf
ENABLE No. 1	10 pf
Output design load capacitance	180 pf
Propagation delay time (50% points)	
Through driver and ENABLE No. 2 inputs	60 ns
Through ENABLE No. 1 input	66 ns
Output transition times (10% - 90%, 180 pf load)	35 ns
Power consumption	
Static operation (both ENABLES low, all driver inputs dc)	0.12 mw
Disabled (both ENABLES low, all driver inputs changing)	3 mW/MHz
Enabled (both ENABLES high, all driver inputs changing)	230 mW/MHz

The power consumption figures represent three different cases which the chip may experience, but do not cover the full gamut of possibilities. The best case is static operation in which the inputs are steady (dc) at either logic level; it doesn't matter which. In this case the only power supply drain is caused by leakage currents which are extremely small and thus entail trivial power consumption. The second case is for both ENABLE inputs low (the disable condition). If the driver inputs switch between their high and low states, some chip power will be required for the charging and discharging of the capacitance load that the input inverters see. The charging and discharging of the input capacitance itself are not counted because that power consumption occurs in the circuit which drives the inverter. The 3 mW/MHz power consumption may be reduced in a linear fashion depending on how many of the driver inputs are switching. The greatest possible power dissipation requires that all three of the following conditions exist simultaneously:

1) all ten outputs are fully loaded to the design load of 180 picofarads; 2) both ENABLE inputs are switching between their high and low states continuously; and 3) all driver inputs are also switching between their high and low states in synchronism with their controlling ENABLE line and with the same polarity as the ENABLE. This dissipation is only 460 milliwatts for 2 MHz operation, which presents no thermal problem for a chip of this size.

The design of the Type A multi-function driver chip evolved through a few variations before culminating in the design described above. They are worth commenting upon because they were presented in the Interim Report, monthly status reports, and in various oral presentations and also to show why they were discarded.

The first approach used a nine-driver chip because at that time the only usable information on the memory chips concerned the 512 x 4 General Electric device which had nine address lines. It also presumed the existence of a decoder on the chip so that higher order address bits could be applied directly to the chip to enable/disable it.

The design approach changed when it was decided to use the RCA 64 x 4 memory device. This initial approach is shown in figure 11, where there are ten driver circuits, six for address inputs, four for chip select, and an on-chip decoder. There is also a common enable line which controls all driver outputs plus the decoder. To satisfy data input and other applications that do not require a decoder, three additional inputs are included which bypass the decoder. Pin limitations (to stay within 24 pins) prevent bringing in four rather than three additional inputs.

Three considerations were principally responsible for abandoning this design in favor of the one chosen: 1) a greater flexibility is achieved by having a driver without decoders, both for the present memory subsystem and for possible future applications; 2) the chip area required for the decoder can be utilized better in enhancing basic driver design and/or improving yield by reducing chip size; and 3) it was found that the decoder circuit could be conveniently placed on a separate chip with other circuits (Type D chip).

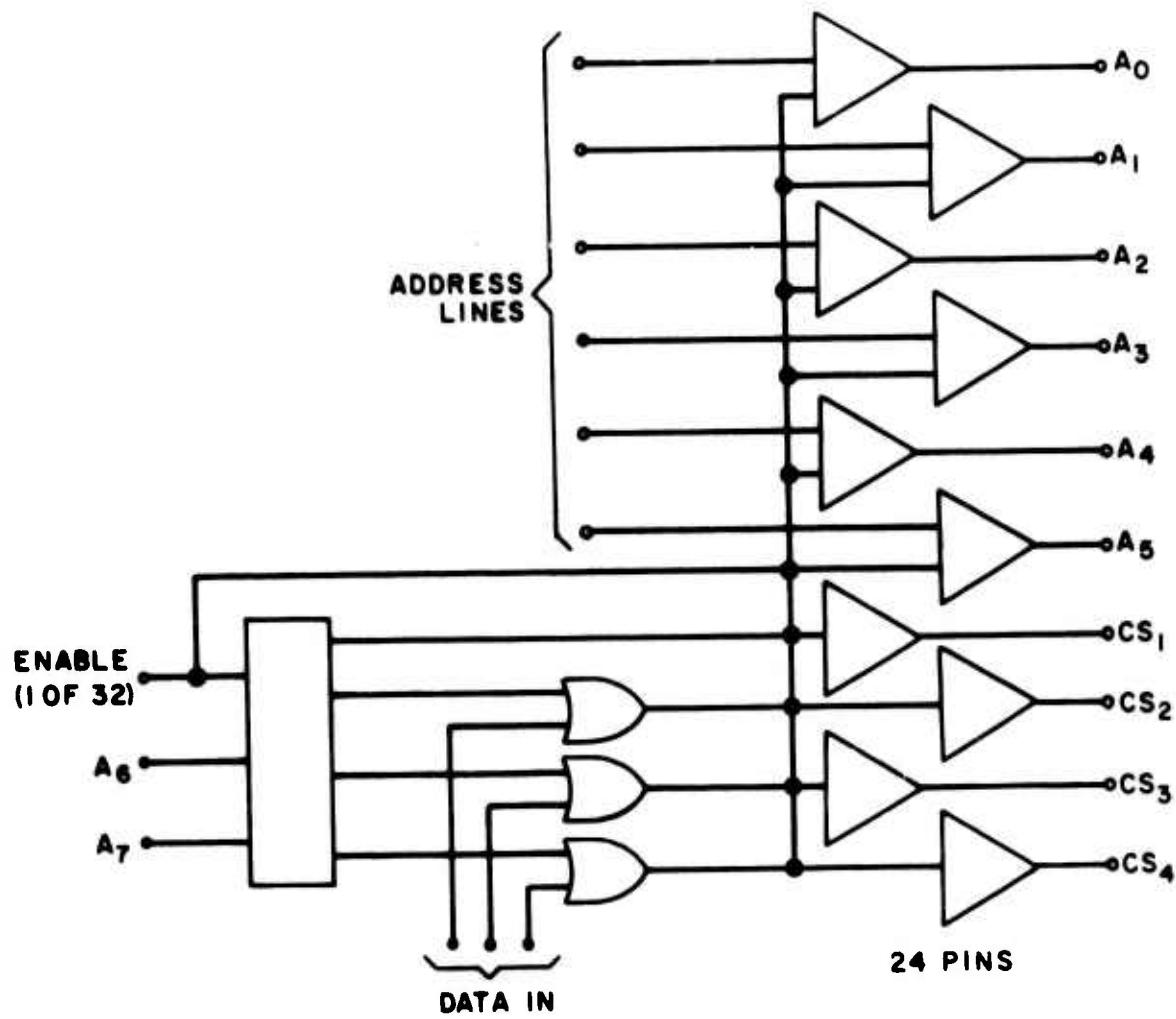


Figure 11. Multi-Function Driver, Initial Design

### C. CHIP TYPE B: DATA OUTPUT BUFFER

The design for the Type B chip is shown in figure 12. It is essentially a 16-input OR gate with an ENABLE and a tri-state output. It is composed of two input gates for radiation considerations as explained in subsection 2E. One of the major constraints involved in the design of this chip is the rather low fanout that is specified for the memory device, viz., 15 picofarads maximum loading. Some of this loading is the capacitance which other memory chip output circuits in the tri-state off condition present in a wire-OR configuration. This tri-state off output capacitance was never specified. One can argue that it should be fairly low because it is generally the junction of one transistor's drain and another's source and these capacitances are small for SOS devices. It would thus seem reasonable to consider that a wire-OR of four memory device outputs, plus the load capacitance of the buffer chip, designed to be small, would meet the 15 pf maximum output loading stipulation. This was the assumption made. One could conceivably go a step further and have a wire-OR of eight memory devices to the buffer chip.

Although the more conservative connection of four was chosen, the design of the buffer chip is such that a wire-OR of eight is completely compatible and would have the advantage of cutting the required number of buffer chips in half.

Because each of the sixteen inputs of a Type B chip is connected to a wire-OR of four rows of memory devices, a single buffer chip provides the readout for a particular bit,  $i$ , from 64 rows in the array (i. e., one half the array). A second buffer chip is required for bit  $i$  of the other 64 rows and the tri-state outputs of these two chips are tied together. Only one of the two may be enabled at any given time via the ENABLE input (active high). In a full 32K x 36 memory (four sections) there will be a total wire-OR connection of eight buffer chip outputs for bit  $i$ .

The buffer is noninverting; a ONE at any input will produce a ONE at the output when ENABLE is high. It is normally impossible for more than one input to have a ONE (high) at any given time because only one row of memory chips is selected at a time and the others are all off (tri-state opens).

However, in a dynamic situation a difficulty arises. It is the case in which a ONE is present at a particular input pin,  $p$ , of the buffer and in the very next memory

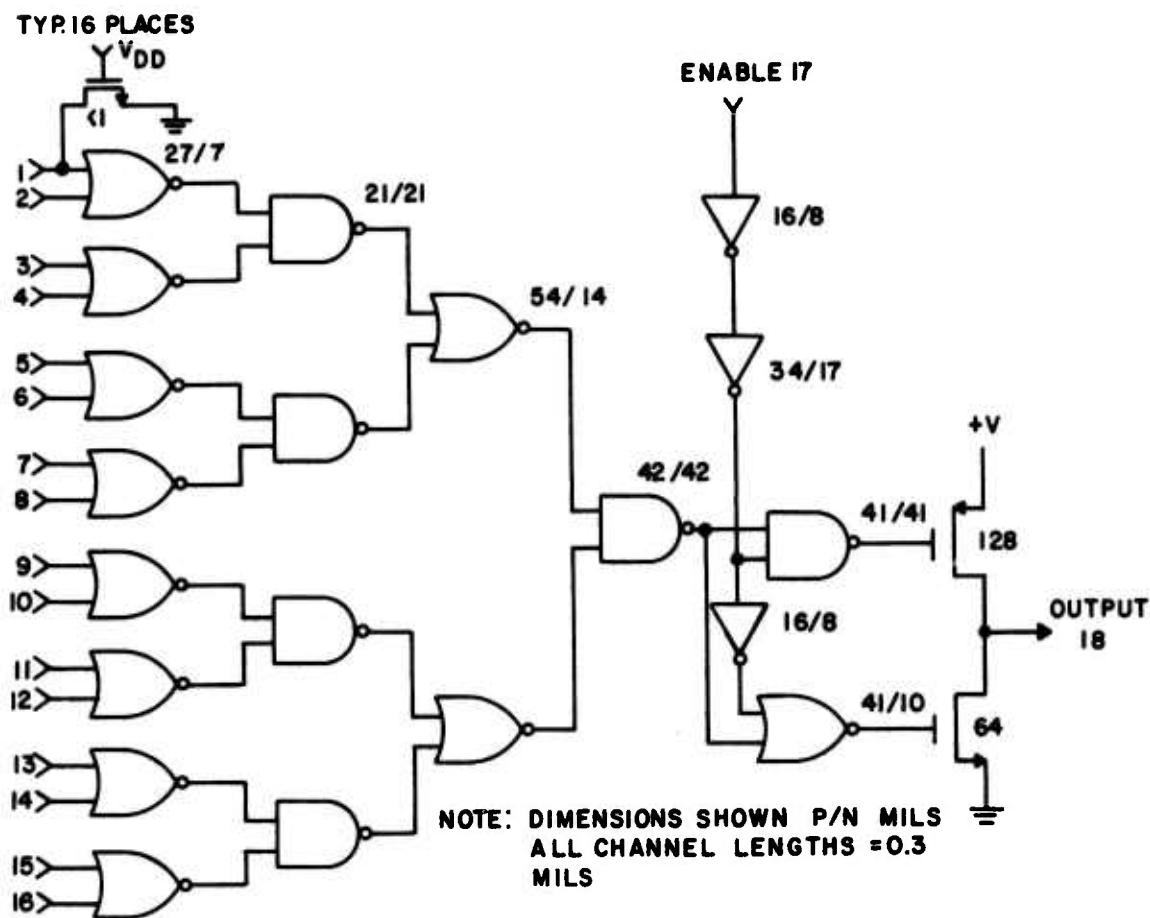


Figure 12. Data Output Buffer, Chip Type B

cycle a ZERO is present at some other input pin, q. All other inputs are tri-state opens. The ONE at pin p persists for some time because the total capacitance at that node sees a very high impedance as soon as the selected row of memory chips becomes unselected (tri-state open circuit). If the ONE voltage is not discharged quickly enough, it will mask the ZERO of the following cycle and cause an erroneous output from the buffer chip. One can calculate what value of resistance is necessary to provide rapid discharge.

Assume that the node capacitance is 15 pf (the maximum load capacitance allowed for the memory devices) and that the memory chip read access time is 200 nanoseconds (which is faster than the RCA memory devices of this program). It is desired then that the resistance sufficiently discharge 15 pf (e. g. to one time constant) in 200 nanoseconds. Using the formula  $\tau = RC$ , one calculates  $R = \tau/C = 200 \times 10^{-9} \div 15 \times 10^{-12} \approx 13$  kilohms. Although it is difficult to fabricate a linear resistance as part of the manufacture of a CMOS/SOS chip, one can make do very nicely with an "MOS resistor", i. e. , an MOS transistor that is biased to be on all the time and whose cell geometry is chosen to present the appropriate resistance. The resistance is nonlinear, being about twice as large when the buffer input is high as it is when the input is low. This is not at all undesirable; in fact it even reduces the dc current drain from a memory chip when its output is high.

As shown in figure 12, the circuit is an n-channel transistor whose gate is tied directly to V<sub>DD</sub> (+10 volts). Such a transistor having a channel width of 1 mil and the standard channel length of 0.3 mil would have a resistance of about 8 kilohms for the high input condition and 4 kilohms for the low. Consequently, the discharge problem can be handled with 16 n-channel transistors of even smaller width (higher resistance).

The impact on chip area caused by including these transistors in the design is clearly very small. There is a current drain of approximately one milliampere required from any memory chip when its output is high which is not expected to present a problem. In addition, there is an extra power dissipation of about 10 milliwatts on the buffer chip whenever one of its inputs is high but, again, only one at a time can be high.

The characteristics of the Type B chip are summarized in table 7.

Table 7

CHIP TYPE B: DATA OUTPUT BUFFER

Function: Routes the selected 1 of 16 inputs to tri-state output with ENABLE/ DISABLE control.

Chip size	100 x 100 mils
Input capacitance	
Data inputs	4.2 pf
Enable input	3.0 pf
Output design load capacitance	50 pf
Propagation delay time (50% points)	
Through data inputs	60 ns
Through ENABLE input	40 ns
Output transition time (10% - 90%, 50 pf load)	20 ns
Power consumption	
Static operation (ENABLE low, all data inputs dc low)	0.03 mw
Static operation (same but one data input dc high)	10 mw
Dynamic operation (ENABLE plus one input at a time switching)	10 mw + 15 mW/MHz

D. CHIP TYPE D: DECODER, GATES AND INVERTER

The basic objective in the design of this chip was to obtain a "catch-all", a chip able to accomplish all other subsystem functions other than driving large capacitive loads and buffering the memory device outputs. This, happily, has been achieved by the design depicted in figures 13 and 14 and in addition, with hardly any unused subsections of chips left over.

The principal part of the chip, in terms of area, is the decoder section. It contains eight output lines and can be used as two separately-enabled 1-of-4 decoders, a 1-of-8 decoder, or as part of a larger decoder. For example, the 1-of-32 decoding necessary to select a particular Type A address/chip select driver is accomplished using

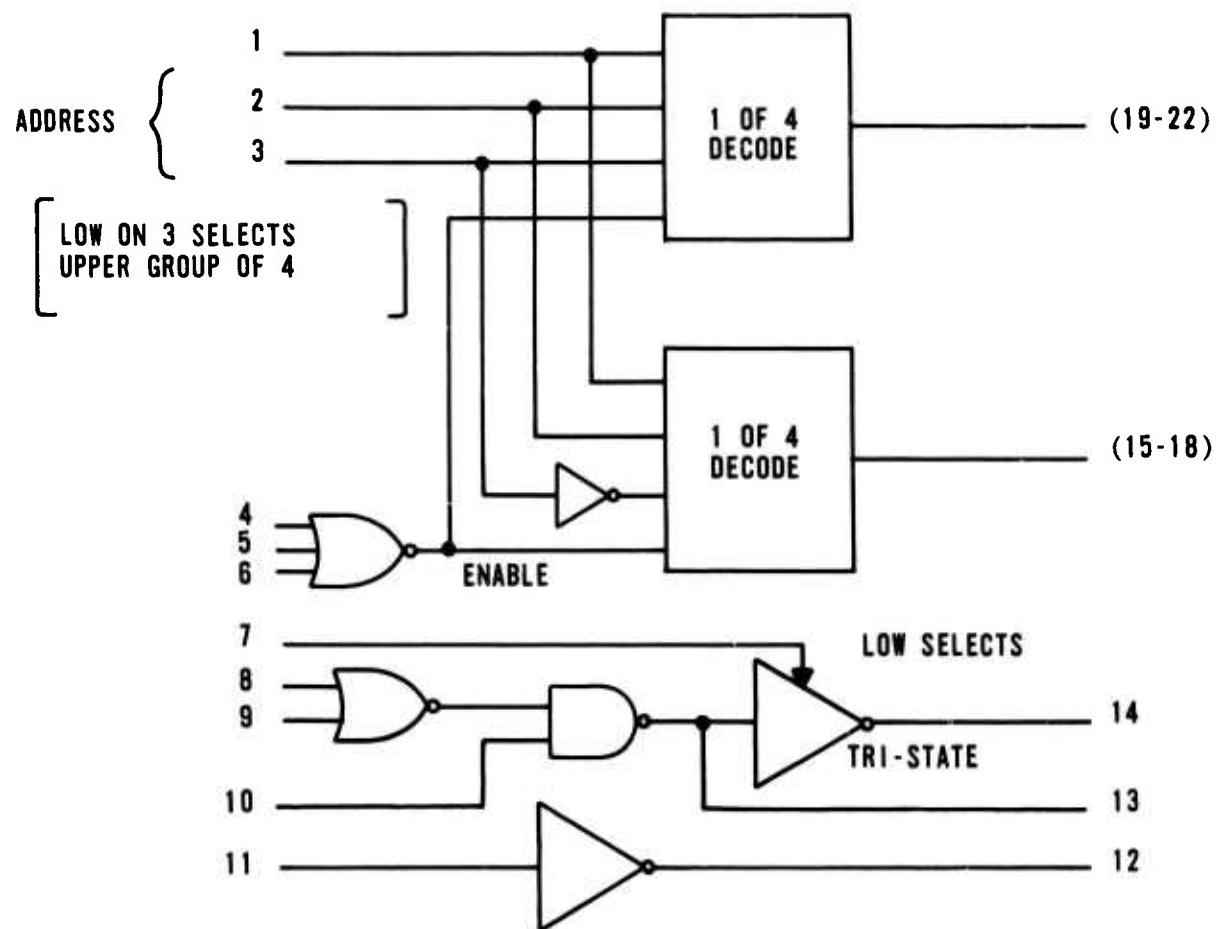
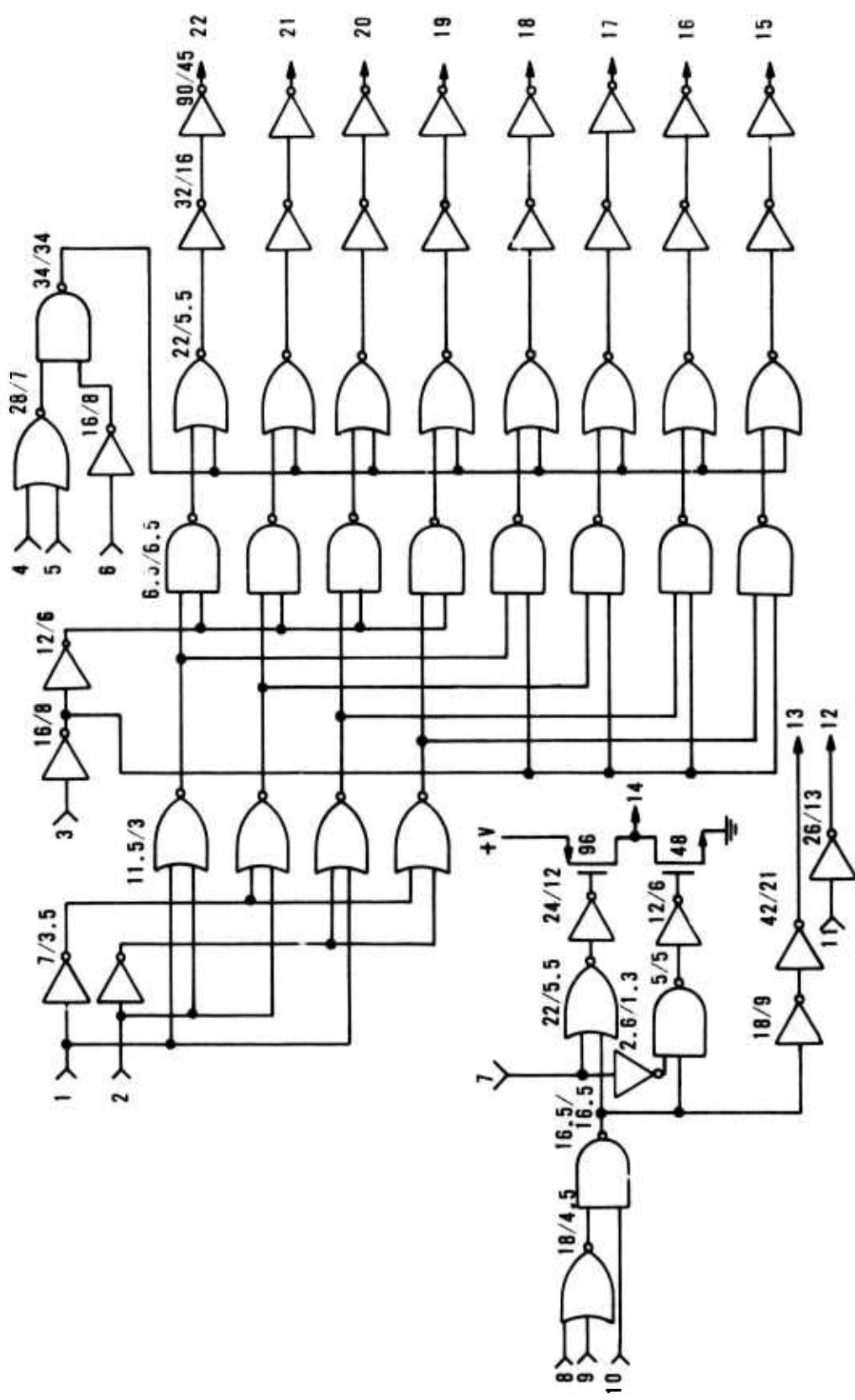


Figure 13. Decoder, Gates, Inverter Device, Chip Type D



**Figure 14.** Type Chip D (Detail)

four Type D chips. One section of memory (8K x 36) requires only eight Type D chips in all. In addition to the decoder section of the chip there is a section with a single independent inverter and another section with two gates and a tri-state inverter. The manner in which these parts interconnect to accomplish system functions is described in Section 3 of this report.

The decoder section is designed so that the selected line is high and all the others low. This permits a direct connection to either of the other two chip types that have active high ENABLE lines. Each output is buffered to permit it to drive a 50 pf load in the specified time.

The chip size is comfortably below the largest attainable at today's state-of-the-art and, hence, space exists to put in heftier output stages to drive even more load. However, subsystem design does not require this and hence the attendant penalties in chip size and propagation delay were avoided by not designing for more than a 50 pf load. The 3-input gate which enables the decoder is actually composed of 2-input gates and an inverter for better radiation resistance (see subsection 2E). The ENABLE condition exists when all three inputs are ZERO (low).

The gates section of the Type D chip provides two separate outputs with the same function. One is a standard inverter designed to drive 25 pf, the other is a tri-state inverter able to handle a 50 pf load. This output is used for those signals which require a wire-OR to the other 8K sections of memory, viz., Address Error and Access Error.

The characteristics of the Type D chip are summarized in table 8.

In addition to the chip logic diagrams, which specify transistor geometries, and the functional specifications, the layout drawings for two typical circuits were generated as part of the contract. They are shown together in figure 15. The large one is the output inverter stage of the Type A chip whose p-channel transistor has a gate width of 192 mils and whose n-channel width is 96 mils. The smaller one is a typical 2-input NAND gate with gate widths of 5 mils. Gate widths vary substantially, as necessary, to accommodate required capacitance gain and loading circumstances.

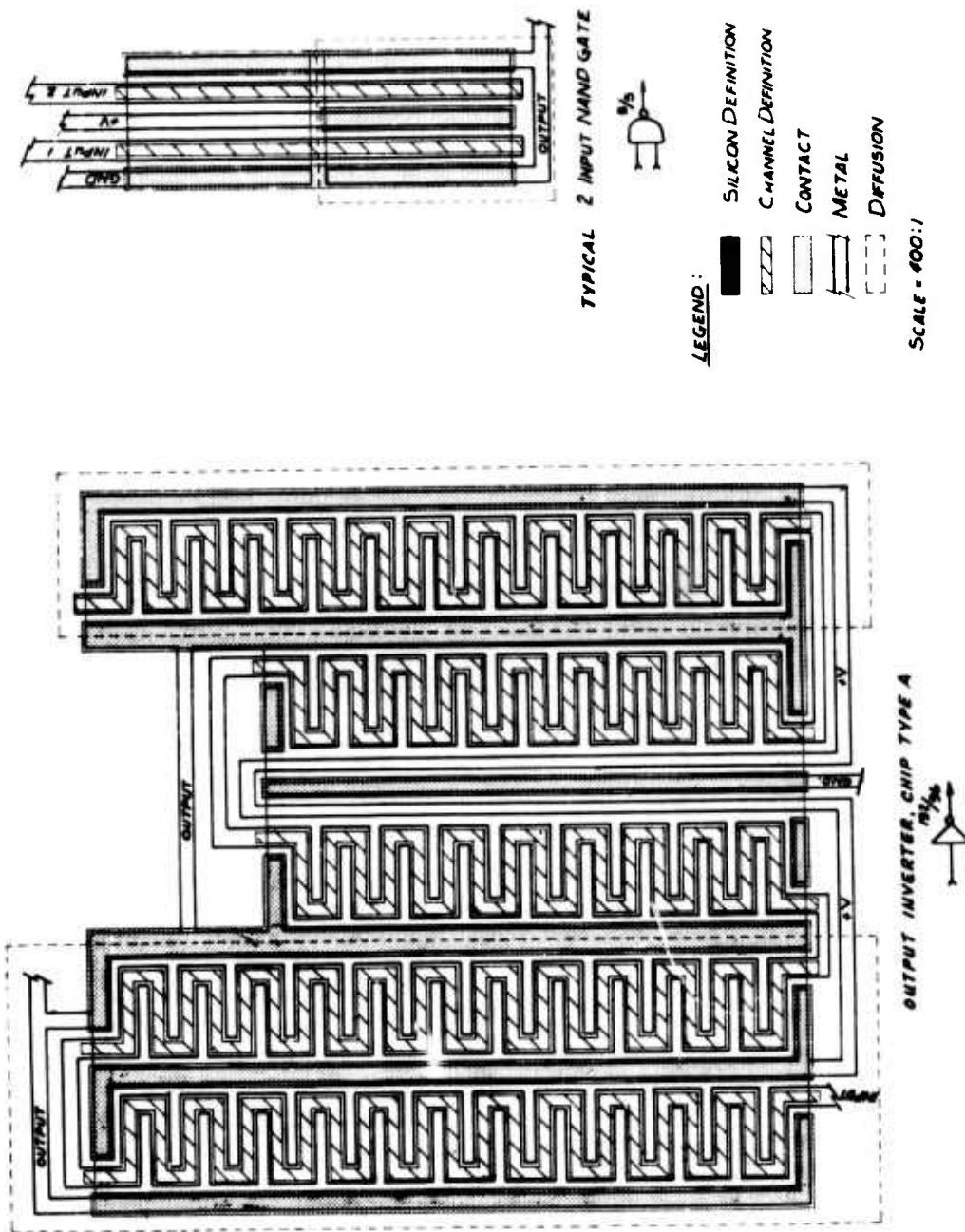


Figure 15. Layout Drawing for Sample Circuits

Table 8

## CHIP TYPE D: DECODER, GATES AND INVERTER

Function: Two 1-of-4 decoders, NOR-NAND gates, inversion

Chip size	125 x 125 mils
Input capacitance	
Pins 3, 6, 8, 9	3 pf
Pins 4, 5, 7, 10	4 pf
Pins 1, 2, 11	5 pf
Output design load capacitance	
Pin 12 (inverter)	15 pf
Pin 13 (inverter which follows gates)	25 pf
Pins 14 through 22 (tri-state and decoder outputs)	50 pf
Propagation delay time (50% points)	
Pin 12 (inverter)	13 ns
Pin 13 (inverter which follows gates)	45 ns
Pin 14 (tri-state output)	55 ns
Pins 15 through 22 (decoder outputs)	75 ns
Output transition times (10%-90%, rated load)	
All outputs	25 ns
Power consumption	
Static operation	0.06 mW
Dynamic operation (all circuits operating)	30 mW/MHz

## E. RADIATION HARDEMENING DESIGN

There are three distinct areas in which a radiation-hardened design may differ from a standard nonhardened design: 1) the types of gates used in the design; 2) the manner in which the gate insulators are fabricated, and 3) the relative geometries of the p- and n-channel transistors in each inverter pair or gate.

In the first area, the necessary precautions have been taken and appear in the designs presented in the foregoing sections. The problem arises because a radiation

environment causes threshold voltage shifts in both p- and n-channel devices. The threshold voltage for p-channel transistors increases whereas that of the n-channel transistors decreases. The resultant effect is to shift the voltage-transfer curve of a gate or inverter. Change of state occurs at a lower input voltage level, thereby decreasing noise margin and increasing over-all propagation delays.

The series-parallel form of CMOS gate circuits accentuates the voltage shift effect in proportion to the number of inputs to the gate. Consequently, the only gates employed in the design are 2-input gates. Requirements for larger gates have been met by stringing together 2-input gates in series.

In the second area of radiation hardening the direction taken is to specify what approaches to gate insulator hardening are considered most promising and then to estimate the effect upon producibility and reliability of fabricating devices in this manner.

Efforts aimed at fabrication and testing necessary to determine specifically what are the best gate insulator hardening approaches are beyond the scope of this contract. Fortunately, Sperry has made such efforts on its Design and Fabrication of Radiation Hardened MNOS Memory Array contract with the Air Force Weapons Laboratory (Contract No. F29601-73-C-0059). This AFWL program has run concurrently with the subject program and is still being worked on. In addition, the literature cited<sup>1,2</sup> provided useful information regarding demonstrated successes which other contractors have had in gate insulator hardening.

The major permanent radiation effects in CMOS/SOS devices are a decrease in transconductance, an increase in leakage current, and changes in the values of threshold voltage. The changes in transconductance are not expected to exceed 20 percent and can therefore be compensated for by design. Changes in leakage currents are

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1. Aubuchon, K. G. , "Radiation Hardening of P-MOS Devices by Optimization of the Thermal SiO<sub>2</sub> Gate Insulator," IEEE Transactions on Nuclear Science, December 1971.
2. King, E. E. , G. P. Nelson, H. L. Hughes, "The Effects of Ionizing Radiation on Various CMOS Integrated Circuit Structures," IEEE Transactions on Nuclear Science, December 1972.

acceptably small, except for those arising from a positive back gate bias in the n-channel device. This effect may be ameliorated by somewhat heavier doping of the p-substrate.

The major processing efforts are concerned with reducing the amount of threshold voltage change for both n- and p-channel transistors. The problem of hardening CMOS gate dielectrics to accomplish this is aggravated because the change in threshold voltage under ionizing radiation must be acceptably small under gate biases of either polarity. The two preferred approaches are: 1) the process developed by Aubuchon which requires a set of special process conditions surrounding growth and treatment of the thermal oxide, and 2) aluminum implantation of the gate oxide.

The major difference between a typical commercial MOS gate process and that developed by Aubuchon is the insistence on the use of the following: (100) orientation of the silicon substrate, oxidation in dry oxygen at 1000°C, the omission of any heat treatment above 800°C, the need for a nonradiative method of aluminum evaporation, and a sintering temperature near 525°C. This process is being followed in detail, with two further improvements: 1) the oxidation is carried out in a cold wall reactor, which guarantees minimum contamination from the furnace walls and 2) the dry oxygen has an admixture of 2 percent HCl, which further guarantees impurity control. This process has resulted in remarkably hard, fixed-threshold voltage gates on bulk silicon. In addition, this gate was used in the fabrication of SOS p-channel and n-channel transistors, whose diffusions and silicon definitions were performed at INSELEK, while gate formation and the completion of processing was done at the Sperry Research Center.

The results of radiation exposure are shown in figure 16, which shows the threshold shifts experienced by p-channel (Aubuchon) transistors during irradiation. Inspection indicates that, under negative bias (normal for p-transistors), the p-transistors performed very well.

Extensive work has established that aluminum implantation will reduce the positive bias threshold voltage shifts of all MOS transistors, which benefits forward-operating n-transistors (and reverse-operating p-transistors). Unfortunately, it also results in an increase in negative bias shifts, adversely affecting forward-operating p-transistors (and reverse-operating n-transistors). This deleterious effect can be minimized by relatively low accelerating voltages, such as 10 keV, with the total density of aluminum not exceeding  $10^{14} \text{ cm}^{-2}$ . In order to utilize the benefits of implantation at

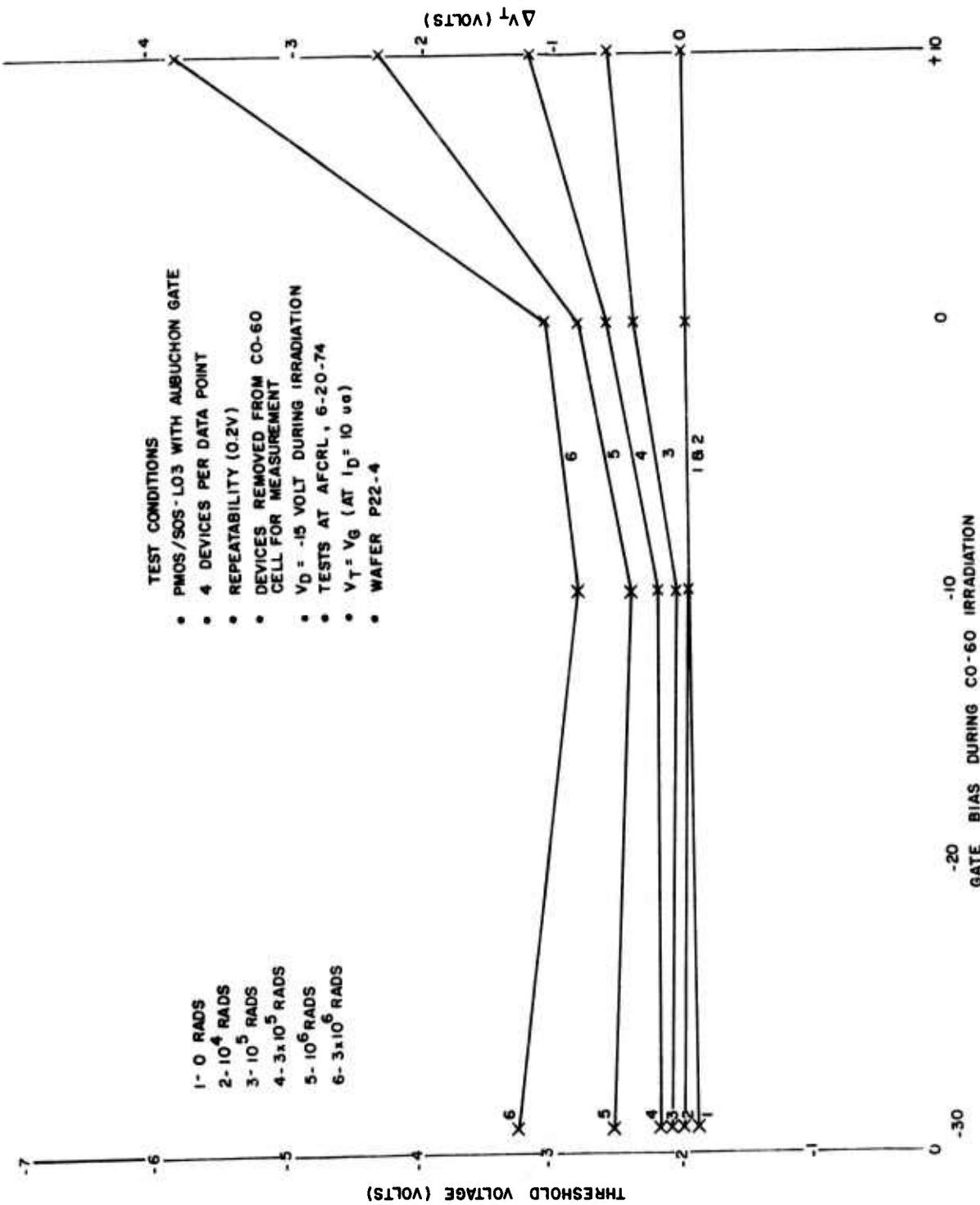


Figure 16. Hardened PMOS-SOS Test Data

positive biases, and avoid deterioration at negative biases, implantation is confined to n-channel devices. Masking against implantation is achieved by a photoresist layer (2-3  $\mu$ m thick) that has windows only over the gates of the n-channel transistors.

If the transistor gates attain opposite-from-normal bias (positive for n and negative for p), unsatisfactory levels of shift may still be experienced. The Aubuchon p-gate (figure 16) at positive potentials clearly shows this. To avoid these conditions, gate voltage clamping is employed. The clamping is achieved by shunting the gate to ground by a diode for both p- and n-channel devices, but only for those circuits wherein the possibility of opposite-from-normal bias exists.

The processing steps outlined above attack the total dose radiation problem but not the transient radiation problem. This is particularly severe because the transient radiation environment specified in the SOW is severe ( $4 \times 10^{11}$  rads (Si)/second). One of the factors which render the situation less difficult is the fact that writing into memory is off-line because it is an EAROM program memory. If this were not the case, circumvention techniques would be required. Even so, the high transient radiation levels require system shielding with a high-Z material. The most vulnerable areas in the memory subsystem are the Type A drivers, because of their large geometry output stages, and the memory chips themselves.

The third area of radiation hardening involves the relative geometries of the complementary p- and n-channel transistors of every inverter or gate. The purpose of altering the standard nonhardened geometries is to raise the switching point voltage above the nominal centered value of +5 volts (for a +10V setting of VDD). In this way the threshold shifts which occur under radiation, and which cause the switching point voltage to decrease, will not carry this voltage as low in absolute magnitude because the starting point was higher than normal. It is not possible to specify precisely how much switching point compensation should be incorporated into the design because gate insulator hardening processes will doubtless continue to improve and further test data will be gathered showing what threshold shifts do in fact occur with the hardened gate devices in various radiation environments. However, one can postulate various degrees of channel width compensation and calculate the effects upon switching point voltage and propagation delay. These calculations have been made and the results are given below.

The essential feature of the radiation compensation is change in the channel conductance of the p- and n-channel transistors in each CMOS pair. For noncompensated design (standard commercial approach) the p-channel width is twice that of the n-channel which gives equal conductances because of the unequal mobilities. In compensated designs the width ratio ( $\alpha = W_p/W_N$ ) becomes even greater. Compensation has no appreciable effect upon chip size because over-all width ( $W_p + W_N$ ) is held constant. The input capacitance of the p-n pair remains unchanged because their gates are connected and load capacitances remain unchanged as they are the input capacitances of following stages.

The switching transients at each node, however, are affected. Rise times decrease (p-channel device going on and n-channel off) because of greater p-channel conductance and fall times increase because of smaller n-channel conductance. A given transient, rippling through a chain of inverter stages, has alternately longer and then shorter transition times. The net effect is an increase in propagation delay relative to the noncompensated design.

In table 9 the percentage increases in propagation time are shown for a) increasing amounts of compensation ( $\alpha = 3, 4, 5, 6$ ) and no exposure to radiation, and b) the same amounts of compensation and an exposure to radiation which changes the p-channel threshold from -2V to -4V and the n-channel threshold from +2V to +0.5V. The interesting cases are for  $\alpha = 5$  and  $\alpha = 6$ , wherein the respective preradiation and postradiation speed values are almost identical, although considerably slower than the reference (commercial design).

The last two columns of table 9 show the percentage changes in the switching point voltage for a CMOS inverter relative to the reference of +5V for a +10V setting of VDD. The effect of increasing amounts of compensation can be seen to be an increasing amount of raising of the switching voltage,  $V_S$ . The most desirable choice here is the  $\alpha = 6$  case because  $V_S$  never gets further than 20 percent (one volt) away from the ideal centered value of +5V. Without any compensation the postradiation switching voltage is quite low: 3.25V (35% below 5V). This reduces noise immunity considerably.

Table 9  
EFFECTS OF  $\alpha$  CHANGES ON PROPAGATION DELAY  
AND SWITCHING VOLTAGE (IN %)

$\alpha =$ $W_P/W_N$	$\Delta t_{pd}$ Pre-rad	$\Delta t_{pd}$ Post-rad	$\Delta V_s$ Pre-rad	$\Delta V_s$ Post-rad
2 (Uncomp.)	REF	25	REF	-35
3	11	27	6	-29
4	25	33	10	-25
5	40	42	13	-23
6	56	52	16	-20

## Section 3

### SUBSYSTEM LOGIC DESIGN AND INTERCONNECTION

#### A. INTRODUCTION

The logic design of the memory subsystem is, for all practical purposes, the design of an 8K x 36 section of memory because of the SOW requirement that each section be able to stand on its own. Referring again to figure 5, one can see that the signals from the computer subsystem are routed in parallel to each of the possible four sections of memory. Signals from the memory are wire-ORed together and then routed to the computer subsystem. Tri-state output circuits are used in each of these wire-OR situations.

The logic design requirements are not demanding ones. In addition to recognizing what mode of operation (read, clear, or alter) the computer specifies and so directing the memory drivers, the only additional requirements are the generation of the Address Error and Access Error signals. As stated in Section 1 the former is generated when an address is specified for which no memory devices exist in a partially populated system. The Access Error is generated when the access mode signals, A and B, are in their nonspecific state, i.e., not read, clear, nor alter. It is not generated, however, if an Address Error exists.

#### B. DETAILED DESIGN

The block diagram of the logic design for an 8K x 36 section of memory is shown in figure 17. All of the gates, inverters, and decoders are shown as individual

symbols. These devices are all on Type D chips and the logic symbol designation indicates which of the eight D chips is involved as well as the pin numbers. In the case of the Type B buffer chips and most of the Type A driver chips, the individual circuits are not shown. Instead, a block symbol is shown which depicts the functional relationship, and the detailed pin connection information is given in backup drawings.

The only factor that distinguishes one section or board of memory from any other is the connection of the Board Enable signal. Address lines A<sub>13</sub> and A<sub>14</sub>, the highest-order bits, designate which board is to be addressed at any given time. Each board, in parallel with the others, decodes these two lines into signals C, D, E, and F (arbitrary letter designations) using one of the two decoders on chip D3. The C line output of board number one is connected by a tray jumper wire to its own Board Enable input and to Address Error circuits of all boards, and the D, E, and F outputs are left unconnected. In similar fashion, the D line output of board number two is connected to its own Board Enable input and to Address Error circuits of all boards, and the C, E, and F lines are left open, and so on with the remaining two boards.

All of the switching of memory chip input lines and, in addition, the switching of the drivers which fan out to the rather large capacitive load presented by the address/chip select drivers, is controlled by the Board Enable signal. Consequently, when a particular board is disabled (Board Enable low) it has very little ac power dissipation - only that of the logic circuits which drive small capacitive loads.

There are many loads that are controlled directly by the Board Enable and Board Enable signals. As a result, the gates and tri-state driver of chip D4 are used, solely for driving purposes. They have an allowable loading of 25 pf (pin 13) and 50 pf (pin 14) compared to only 15 pf for the inverter on the D chip. The NOR gates, decoders and tri-state drivers require a low signal to be enabled and are thus connected to Board Enable. The tri-state driver which provides this signal (D4 pin 14) is always enabled by the ground connection to pin 7.

It is worth noting that the logic symbol designations in figure 17 for the gates/ tri-state driver section of the D chip are simplified versions of the actual logic depicted in figure 14. For example, the NAND gate output (pin 13) is not taken directly from the gate but is buffered by two inverter stages. In addition, the tri-state inverter is not a simple two-transistor inverter but a more complex circuit.

The Address Error logic circuits are in the upper left hand corner of figure 17. The memory subsystem tray wiring is such that the C input (D1-8) of all boards is connected to the C output (D3-22) of board number one, the D input (D1-9) of all boards is connected to the D output (D3-21) of board number two, and so on. The logic will keep the Address Error line low as long as one of the four inputs (C, D, E, F) is high. However, if they are all low, Address Error goes high, indicating a problem. This would occur, for example, in a memory with only three boards (sections) and A<sub>13</sub> and A<sub>14</sub> both high. Decoded output F (D3-19) is then high but this signal is not available from the missing board four and the Address Error logic sees all low inputs.

The Access Error logic circuitry is depicted immediately below the Address Error logic. It simply notes the 1, 0 condition of access mode signals A and B causing the Access Error line to go high, unless the existence of an Address Error blocks this via the connection from D2-13 to D3-10.

The proper timing of memory subsystem operations in read, clear, and alter cycles is accomplished by the use of the Memory Strobe signal. Its connection through the D3 inverter to decoder input D1-6 affects the turn-on times of the clear, read/write, and data input drivers. Its connection to D5-10 and the ensuing logic affects the turn-on times of the two ENABLE lines for the output buffers. There is an additional timing signal available at the computer-memory subsystem interface, viz., "Input Clock". This signal was not found necessary for controlling memory subsystem timing and hence was not used.

In addition to the logic circuits involved in the foregoing areas it is necessary to use a few inverters for generating the notted condition of address lines A<sub>11</sub> and A<sub>12</sub>. Inverters are not used, however, as a general procedure on all inputs from the computer subsystem for load buffering. This is because the allowable capacitive loading by the memory subsystem was not specified in the SOW.

In the event that only a very small loading is permissible, buffers would be required in many places. The most significant of these places, numerically, is the data input area (36 lines). In the subsystem as depicted, each data input line goes to four Type A driver inputs (3.4 pf, each) giving a capacitive loading of about 14 pf per board and about 56 pf in a full four-section memory.

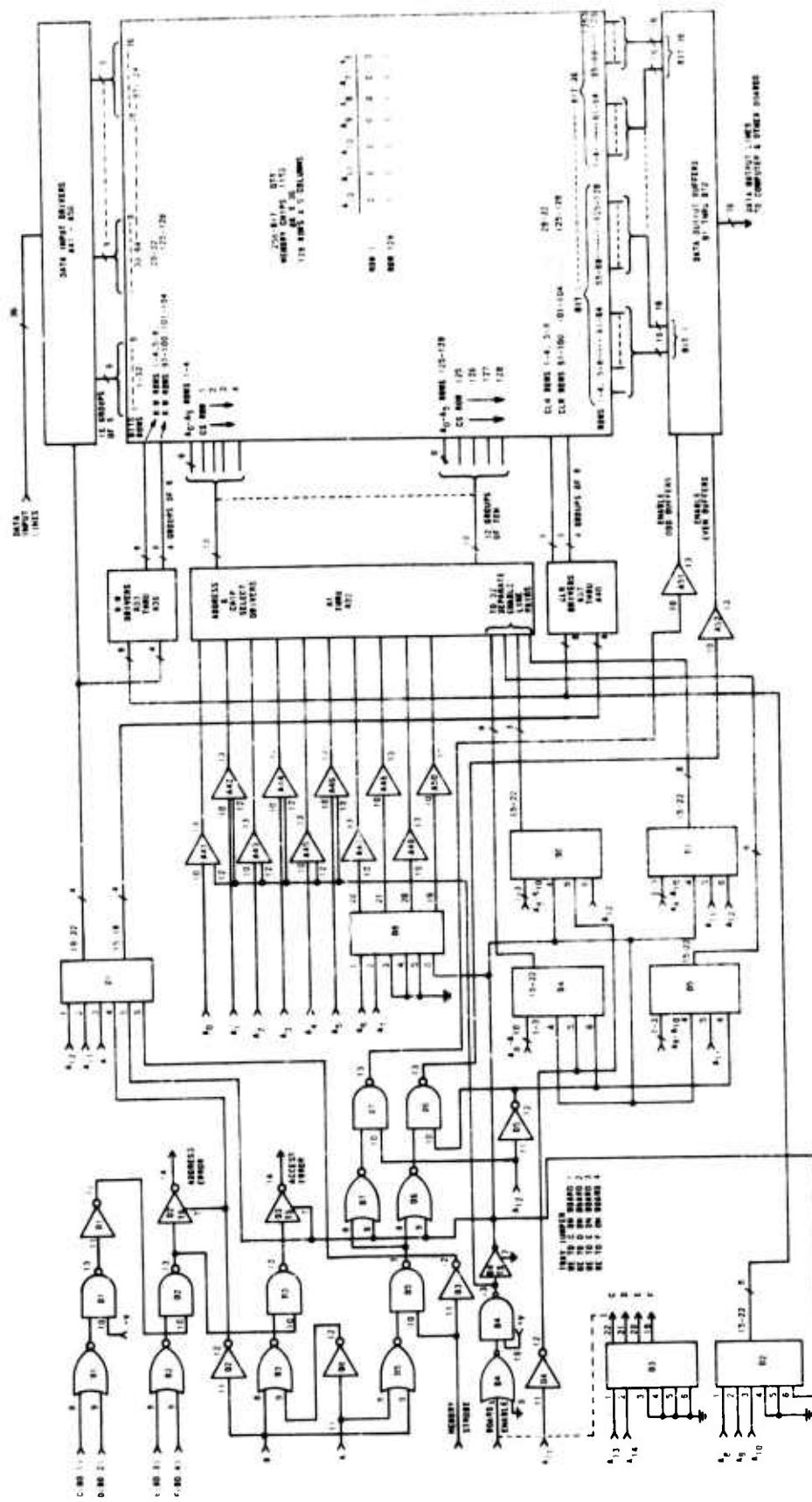


Figure 17. Logic Diagram. 8K x 36 Section

If inverters were used to reduce this capacitive loading one would certainly not want to use Type D chips, as only one inverter (or at most two, if the gates are also used) per chip is available. One could use Type A chips to obtain 10 buffer circuits per chip, although these circuits are overdesigned for these applications and hence are overly expensive.

The only remaining alternative is the creation of a fourth chip type. Although this is surely something to keep in mind and the design is not likely to be difficult, it has not been done on this program, primarily because of the absence of a clearly established need for it.

The decoders on the Type D chips are used in several different fashions. The decoder section of chip D2 is employed as a 1- of -8 line decoder in conjunction with the Type A drivers for the Clear and Read/Write memory chip inputs. It is desirable from a power dissipation standpoint not to apply these signals simultaneously to the entire memory array, but rather to confine their turn-on to the selected row of memory, or some small number of rows that includes the selected row. In this case, the small number is four, based upon the ability of the Type A driver circuit to drive four rows' worth of capacitance (180 pf).

Figures 18 and 19 show the manner in which decoder D2 is used. In each case, four A chips are employed with eight of their 10 driver circuits utilized. Each of the eight outputs of the D2 decoder is connected to the corresponding driver circuit in each of the four Read/Write driver chips and each of the four Clear driver chips. Thus, four of the 32 driver circuits used for Read/Write (or for Clear, when so designated) will tend to be active. However, the additional control of the ENABLE lines of the Type A chips by decoder D1 allows only one circuit in the group to be active at any time.

The D1 decoder section is operated as two 1- of -4 line decoders. One of these (output pins 19-22) is activated by the access mode signal combination which designates a Write or Alter operation. The same four lines are used to ENABLE one of the four R/W driver chips and one of the four sets of data input driver chips. The other 1- of -4 line decoder (output pins 15-18) is activated by the access mode signal combination for a Clear operation.

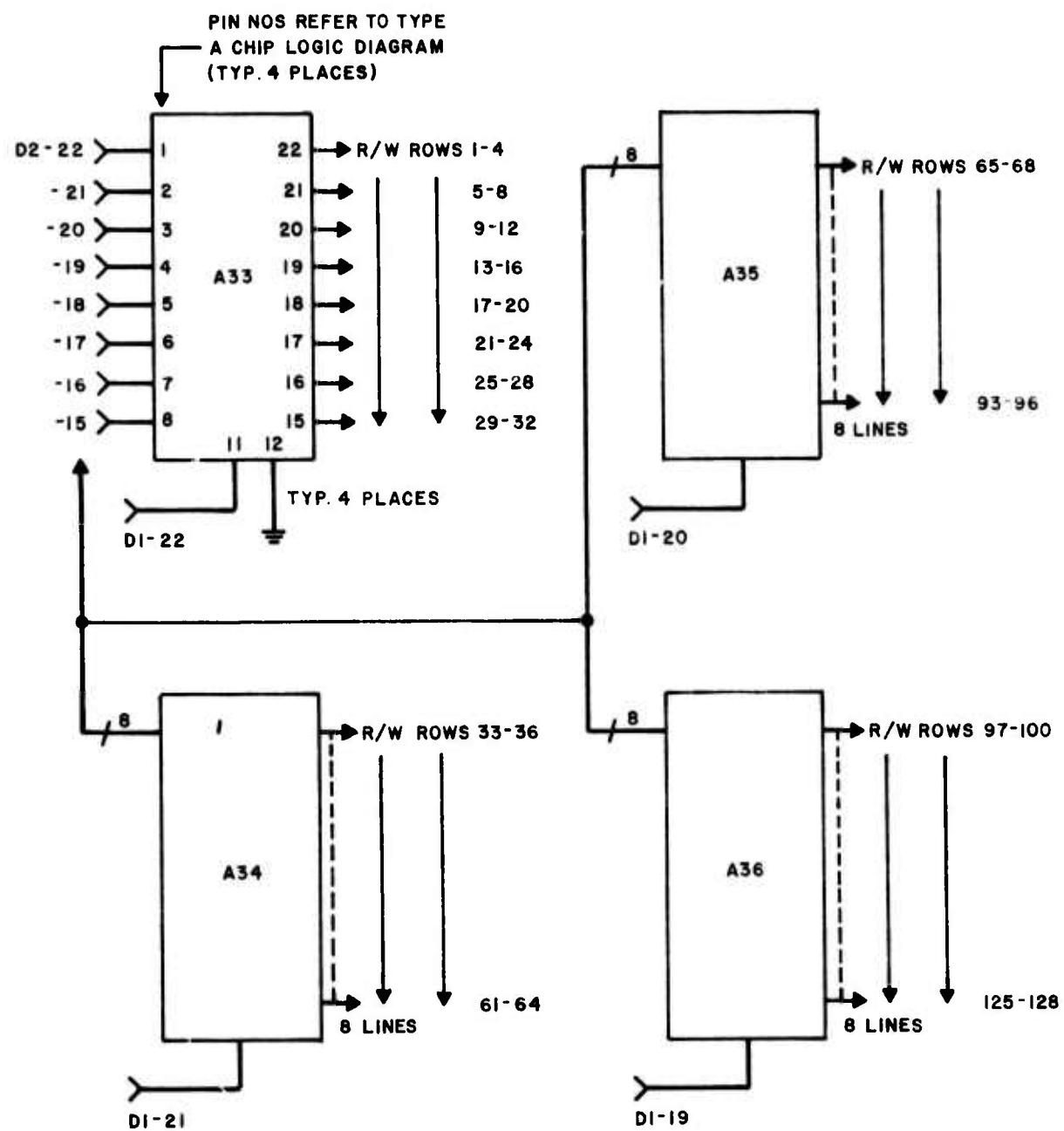


Figure 18. Read/Write Drivers Interconnection

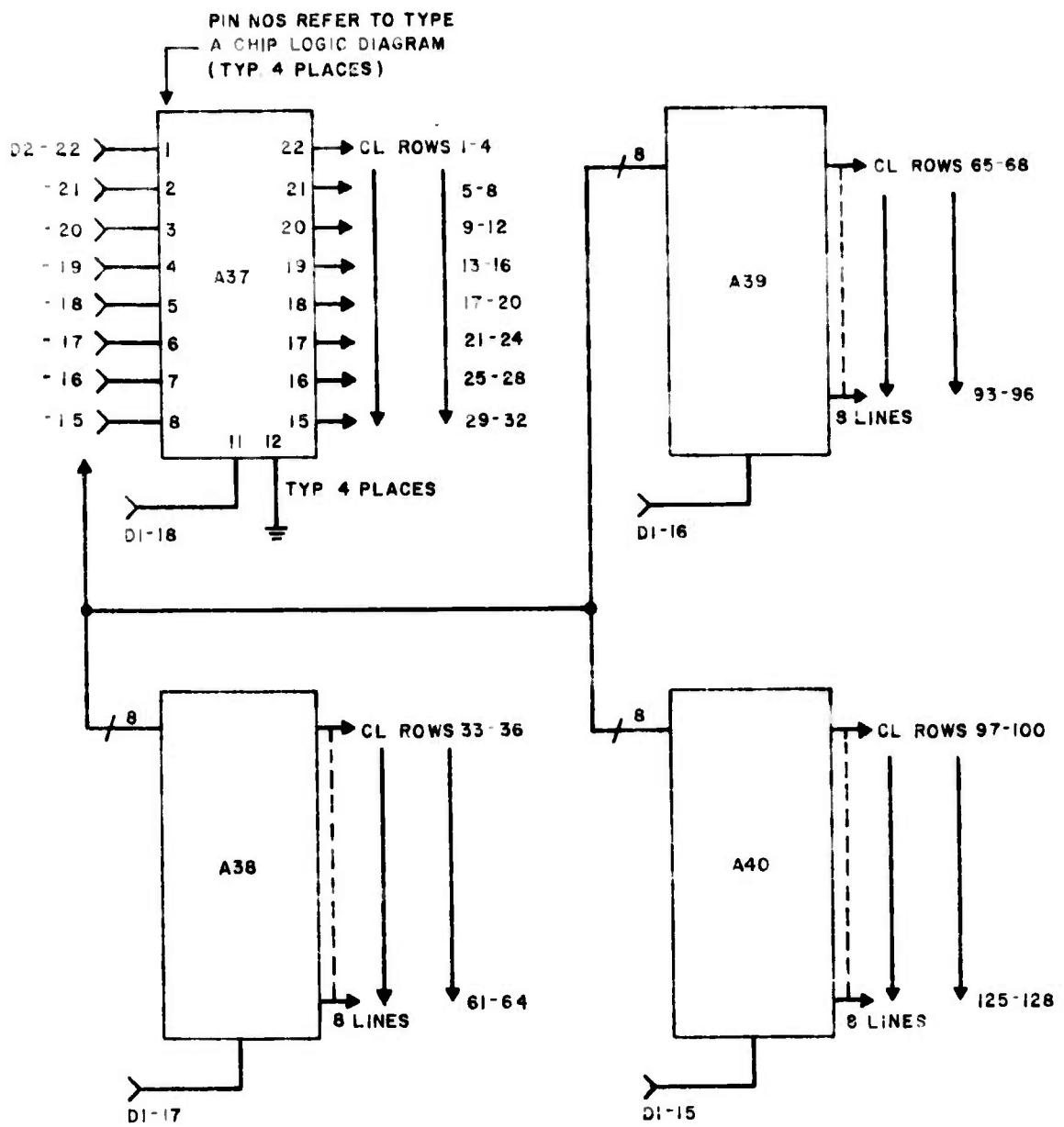


Figure 19. Clear Drivers Interconnection

Only one of the two 1- of -4 line decoder sections of chip D8 is used. It decodes address lines A<sub>6</sub> and A<sub>7</sub> to select a particular row of memory in each successive group of four rows. The four outputs (pins 19-22) must each fan out to 32 Type A driver circuits and, hence, require buffering. The buffering is done by additional Type A circuits, which are spare circuits on the data input driver chips.

The manner in which drivers A1 through A32 drive the address and chip select lines is shown in figure 20. This figure also helps to clarify the manner in which the remaining four decoders D4, D5, D6, and D7 are employed. The control and address lines into these four chips are such that the eight output lines of each combine to form a 1- of -32 line decoder. Each of these 32 lines is connected to the common ENABLE 1 and 2 lines of a single Type A chip. The result is that only one of the A1 through A32 chips is enabled, thereby providing A<sub>0</sub> through A<sub>5</sub> driving to four rows of memory chips and chip select driving to the selected one of those four rows.

The manner in which the data inputs are accommodated is shown in figure 21. The 36-bit word requires at least four driver chips with nine of their 10 circuits employed. When the capacitive load (at 5 pf per memory chip input) is considered, relative to the driver's design load of 180 pf, a four-part split of the memory is dictated. This means that each driver circuit handles 32 rows, i.e., 160 pf.

The power dissipation situation produced by this arrangement is unfortunate in that only one of the 32 rows requires the data input information at any given time. However, the alternative is a larger number of driver chips with lighter capacitive loading on each. This is considered even more undesirable, especially because the memory is a program memory and writing into it is, presumably, an infrequent occurrence.

The manner in which data outputs are handled is illustrated in figure 22. The fact that each buffer chip handles the outputs of a particular bit from 64 rows of memory, and the reasons behind this, were explained in subsection 2C. There are two ENABLE lines, each of which drives half of the buffers (i.e., 36) for a loading of 180 pf. The A<sub>12</sub> address line is the factor that determines which buffer enable line is high. The odd-numbered buffers, which service the upper half of the memory array, are enabled for A<sub>12</sub> = 0, and the even-numbered buffers are enabled for A<sub>12</sub> = 1. Of course,

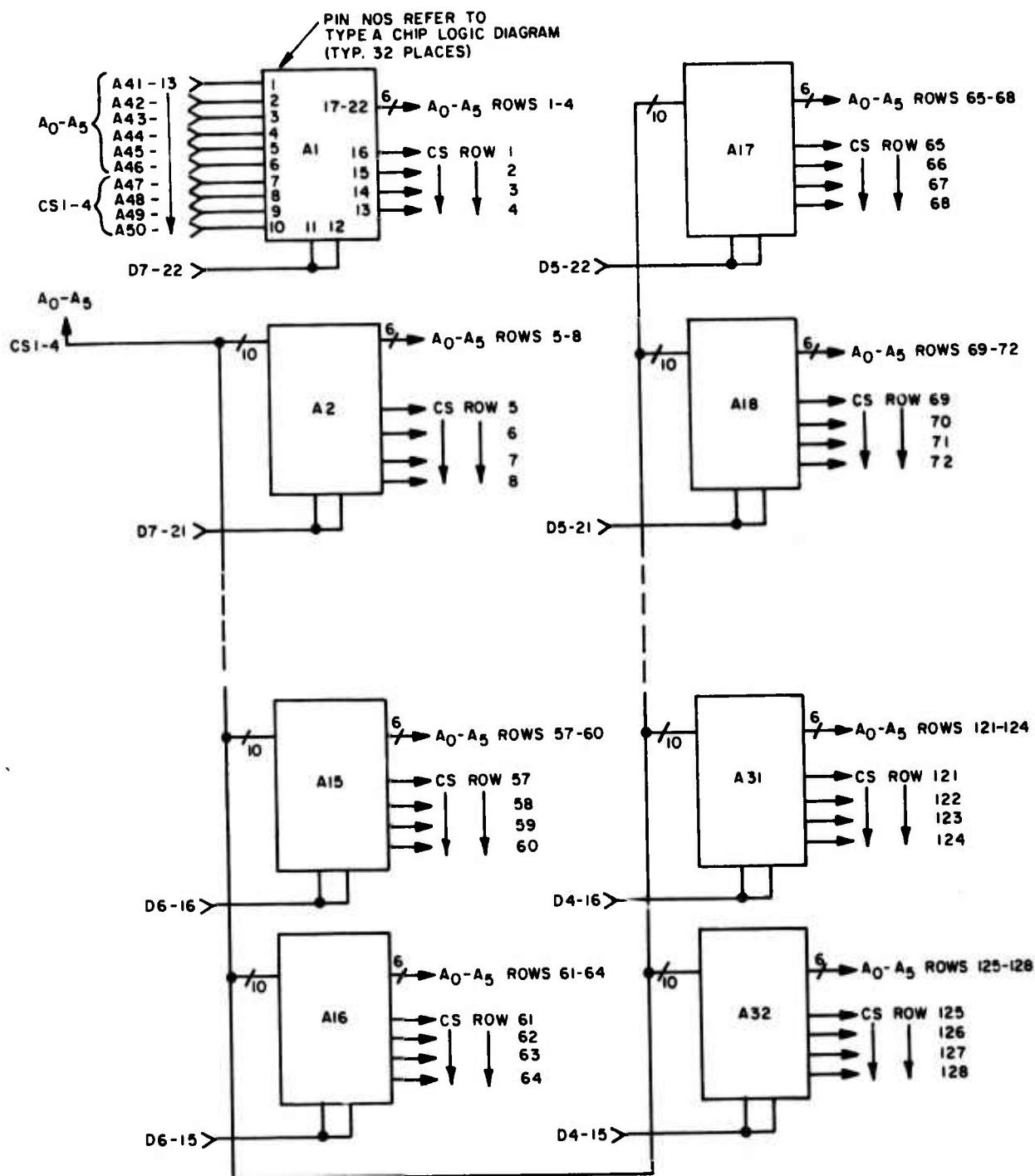
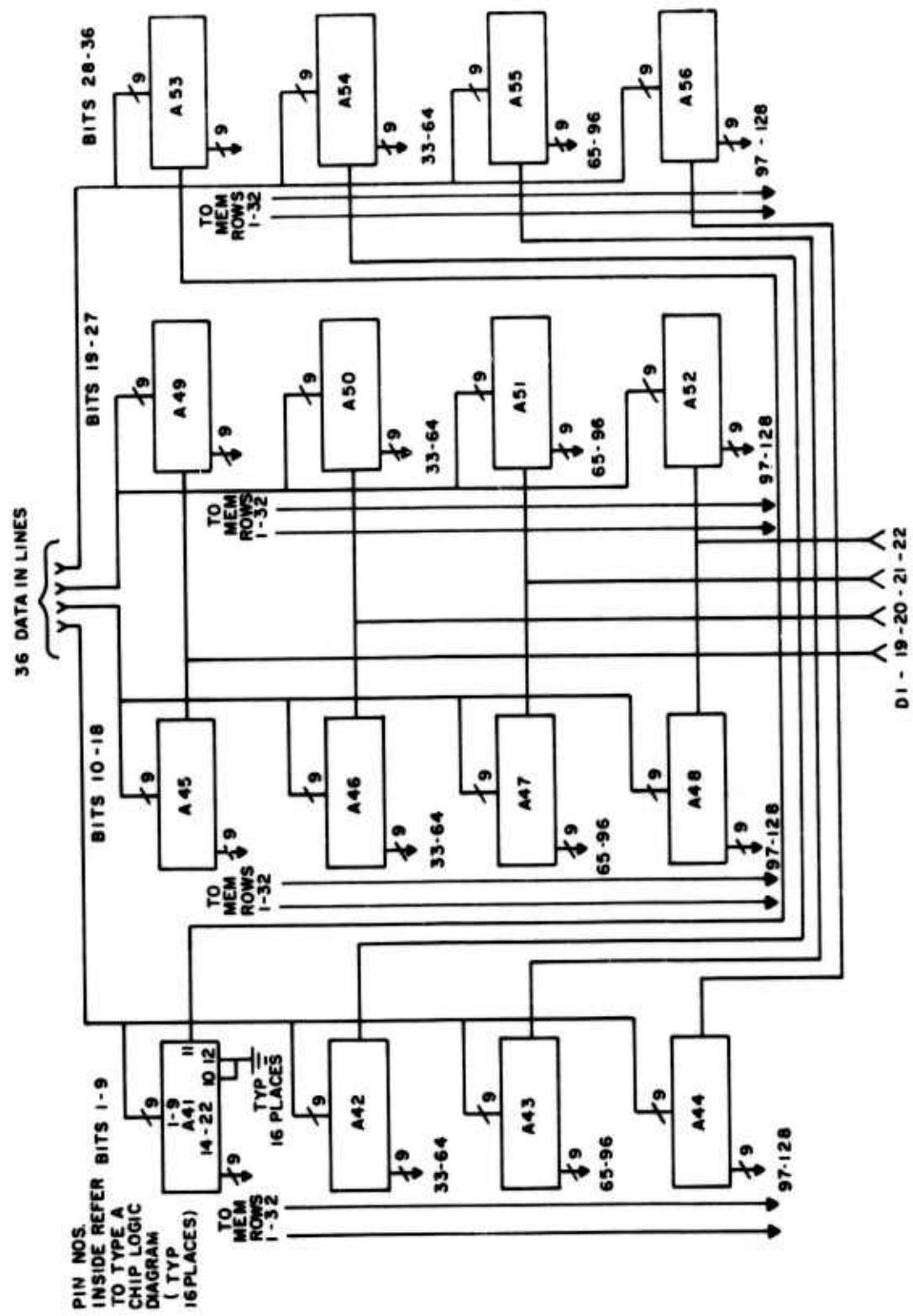


Figure 20. Address/Chip Select Drivers Interconnection



**Figure 21. Data Input Drivers Interconnection**

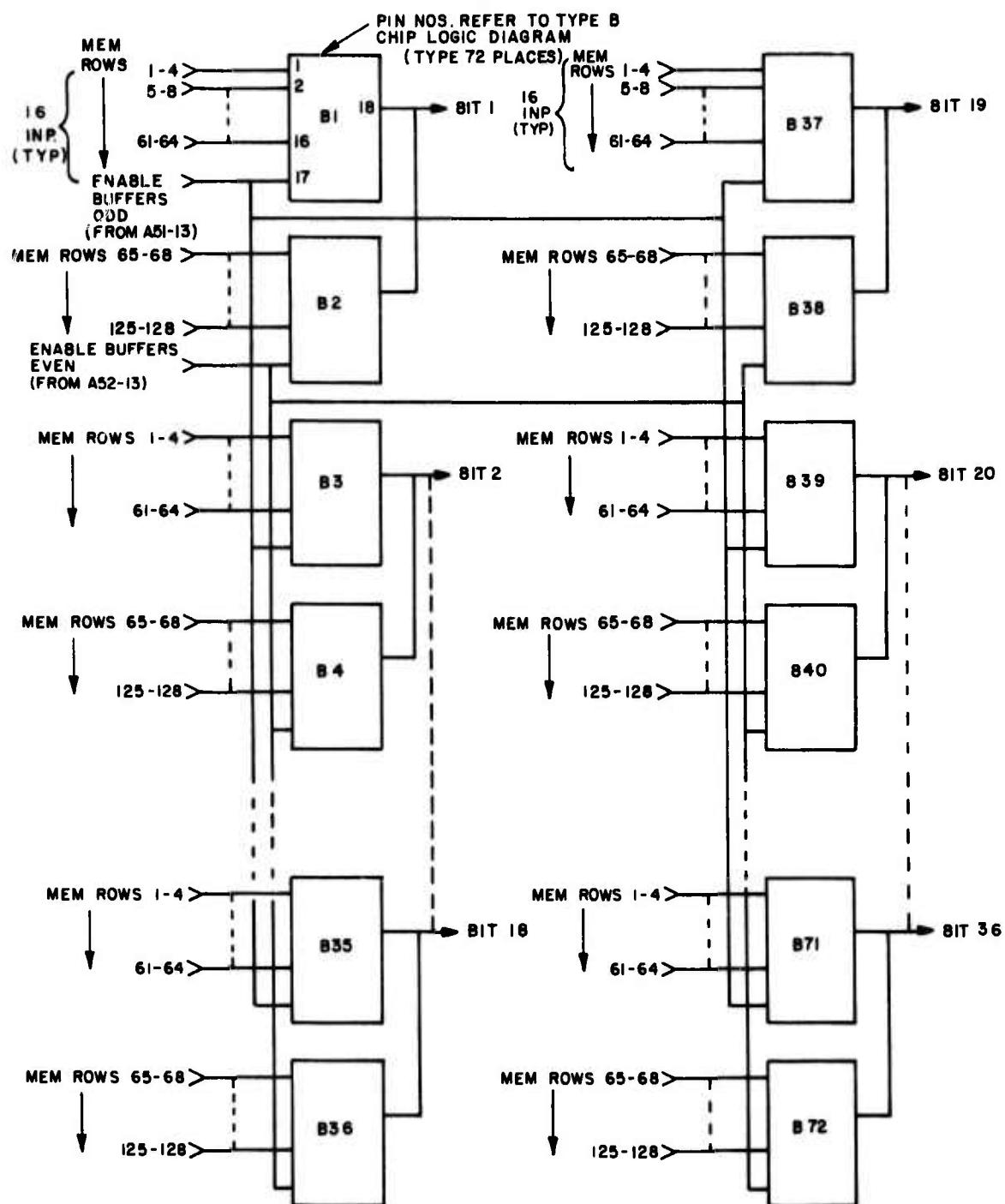


Figure 22. Data Output Buffers Interconnection

neither group is enabled if Board Enable is low, or if the memory is not being exercised (Memory Strobe is low).

The numbers of chips in a single section of memory are as follows:

CHIP TYPE	QUANTITY FOR 8K x 36 SECTION
Memory (64 x 4)	1152
Type A: Multi-function driver	56
Type B: Data output buffer	72
Type D: Decoder, gates, and inverter	8

Two significant observations can be made regarding these numbers. One is that the number of control chips, 136, is less than 12 percent of the number of memory chips, an extremely small amount.

The percentage of overhead control chips for popular commercial MOS dynamic memories, such as the 1103 1K RAM and the recent 4K RAM's, is substantially larger, generally over 50 percent. Two factors that influence the 12-percent figure strongly are: 1) the relatively small size of the memory devices, which tends to make the overhead percentage low, and 2) the conservative assumption made regarding the extent of wire-ORing which is feasible at the memory chip output pins. This conservative assumption (a wire-OR of only four chips) resulted in 72 Type B chips. A less conservative assumption (a wire-OR of eight chips) would result in 36 Type B chips and a total overhead of less than 9 percent.

### C. POWER DISSIPATION

The power dissipation of the memory subsystem can be calculated approximately. Chip power dissipation figures were given in subsections 2B, 2C, and 2D for various conditions of operation. For the dc situation, the power dissipation for an ideal CMOS circuit is zero, as either the p-channel or the n-channel transistor is off at any given time.

Leakage currents do exist, however slight. The approximation for leakage current flow used in the calculations was 5 nanoamperes per mil of channel width of the off devices. Wherever it was not clear whether the p-channel or the n-channel

device in a particular CMOS pair was off, the average of the two channel widths was used in the calculations. The "MOS resistors" used on the Type B chip to discharge input node capacitance actually affect the dc power dissipation to a greater extent than leakage currents, as will be shown below.

For ac power dissipation the charging and discharging of node capacitances was considered. These capacitances are the loads seen by the various devices, and also the internal on-chip capacitances which were calculated as part of the design of the three chips.

The formula for the power dissipation is  $CV^2f$ , where C is the node capacitance, V is the voltage (assumed to be 10 volts), and f is the frequency. Although the ac dissipation figures for the chips themselves were given in terms of milliwatts per mega-Hertz (mW/MHz), the totals calculated for this section are based upon 2-MHz operation because the SOW requires a 500-nanosecond read cycle time.

Consider first the power dissipation of the Type A chips. Even with the calculated values for power dissipation for the three cases chosen, one cannot calculate exactly the over-all power dissipation for the subsystem complement of Type A chips. This is because the enabling/disabling of the chips depends upon address sequencing. However, since the memory is a program memory, the approximation that addresses are always used in exact numerical sequence may be taken.

In this situation one address driver chip will be enabled for 256 successive addresses (4 row x 64 words/row) and all of the others will be disabled during that time. For the enabled driver chip, only the least significant address line will switch on and off at the read cycle rate and the remaining five will switch at 1/2, 1/4, 1/8, 1/16, and 1/32 of that rate. The four chip select lines will each switch at 1/64 of that rate. In such a case the selected chip will dissipate only about 90 mW for 2 MHz operation, i.e., a read cycle time of 500 nanoseconds.

During the time this selected chip is enabled, the other 31 address driver chips will all be disabled, dissipating about 0.6 mW each as they experience the same address sequencing changes as the selected chip. This adds an extra 20 mW (31 x 0.6, rounded off), bringing the cumulative dissipation to 110 mw.

In addition to the 32 address line and chip select driver chips, one must include the 10 driver circuits which drive the load presented by these chips. These 10 driver circuits are enabled at all times, during which the particular section of memory (8K words) is being exercised. They would therefore dissipate the same 90 mw as the selected address/chip select driver, except that their load is about 110 pf each ( $32 \times 3.4$  pf) rather than 180 pf. This reduces their dissipation proportionately to 55 mw, bringing the cumulative sum to 165 mW.

In addition to the address/chip select drivers and their source line drivers, the Type A chip is used for data input, read/write, clear and for the enable lines of the data output buffers. However, for normal on-line program reading the first three areas of application are not exercised; there is no clearing or writing, and no data input line usage. Consequently, although these devices do consume power for the occasional alteration of the stored program, it is not of consequence as long as worst-case dissipation for the chip itself is never excessive - and this has already been demonstrated.

The last area of application is the output buffer enable lines. The power consumption here is trivial in normal address sequencing because each enable line is on for 4096 consecutive addresses; effectively, they hardly switch at all.

The power dissipation calculations for the 72 Type B chips depend very much upon what one assumes for the data word that is read out of the memory and also upon the address sequencing. The dissipation figures listed for the individual chip in subsection 2C are worst-case and certainly should not be multiplied by the number of chips to arrive at realistic over-all dissipation numbers. The following assumptions, believed conservative, will be made to calculate the power dissipation for the Type B chips: 1) the average number of ONES in a data word is 24 (2/3 of the word length); 2) address sequencing through the memory is predominantly consecutive and thus the buffer enable lines switch at a very low rate; 3) on the average, each bit line will change to the opposite polarity in subsequent read cycles two-thirds of the time. Under these conditions the dc power dissipation will be 240 mw because the 24 ONEs will each produce a 10 mw dissipation in the discharge "resistors". The ac power dissipation for the designated conditions is about 12 mW/MHz for each buffer circuit. For 36 circuits,

2 MHz memory operation and a 2/3 factor for bit polarity change the ac power dissipation is 576 mW. The total for the Type B chips is thus 816 mW (576 + 240).

The dissipation for the eight Type D chips is the hardest of all to calculate because of the divergent ways in which the chips are used and because not all sections of all chips are used. Again, the multiplication of the worst-case dissipation per chip by the number of chips would give a dissipation value far above the actual. It is best to work from the logic diagram (figure 17) and determine which circuits switch at what rates and with what capacitive loading, on chip and off. Using the same ground rules employed for the other two chip types, i. e., consecutive address sequencing and read only operation, it quickly becomes evident that the circuits involved switch at very low rates. All of the decoder circuits involve higher order address bits. Decoder D8, the most frequent switching unit, responds to changes in address line  $A_6$ , which switches at 1/64 the rate of line  $A_0$ . In addition the access mode signals do not change at all for read only operation and thus an Access Error would not occur. It is also considered rare for an Address Error signal to occur. Without going into excessive detail, it is fair to conclude that dissipation on the Type D chips is insignificant compared to the totals accumulated for the Types A and B chips and hence only a token value will be assigned to round off the final result.

The calculations for power dissipation in an 8K x 36 memory subsystem show the following results, exclusive of memory chip power dissipation, which was not specified during the program.

<u>CHIP TYPE</u>	<u>CALCULATED DISSIPATION IN NORMAL SYSTEM OPERATION (mW)</u>
A	165
B	816
D (token value to round off)	19
	<hr/>
	1000

This calculated value of one watt compares very favorably with the requirements of the SOW which specifies that the average power shall not exceed 5 watts, with a goal of 1 watt. This is specified for a 2K x 36 subsection of memory, whereas the calculated results apply to an 8K x 36 section. However, the SOW also specifies that the maximum average power drain from the +10 volt supply be 250 mW. This

requirement clearly has not been met, even disregarding whatever the memory chips may draw on the +10 volt line. The value of 250 mW is considered much too low and it is hoped that more power could be allocated.

The static (nonoperating) power dissipation of the elements in the 8 K x 36 memory was not included in the dynamic power calculations because it is so small. By way of contrast to the operating dissipation, it is interesting to consider what the completely static dissipation (no devices switching) would be. In this case, the number of chips of each type can be multiplied by the static dissipation number for that type and the totals added. The results are:

<u>TYPE</u>	<u>NO. CHIPS</u>	<u>mW EACH</u>	<u>TOTALS (mW)</u>
A	56	at 0.12	6.7
B	72	at 0.03	2.2
D	8	at 0.06	0.5
			<u>9.4</u>

This extremely low standby dissipation is, of course, one of the most attractive aspects of CMOS circuits. In considering the operating power dissipation of the full configuration memory (32K x 36), it becomes clear that it is very close to the operating dissipation of one 8K x 36 section, because the nonoperating sections, whose Board Enable signals are low (disable condition), consume essentially only the standby power, again disregarding whatever power dissipation occurs in the memory chips themselves.

#### D. PACKAGING

The requirements for packaging given by the SOW may be summarized as follows:

- 8K x 36 memory subsystem to be mounted on one epoxy board measuring no more than 8.6 x 9.0 inches
- All components, except for discrete components, shall be in flat pack modules

- Components shall be mounted on one side of the board by welding and interconnections made by wire welds on the reverse side
- Boards shall have center-to-center spacings in the subsystem of no more than 0.5 inch

During the course of the contract the bit capacities of both the GE and RCA memory chips were reduced below the sizes specified in the SOW. The selected device (RCA), with a 256-bit capacity, requires that 1152 memory chips alone be used for each 8K x 36 section of memory. This makes the attainment of the packaging goals of the SOW a manifest impossibility. Two alternatives come to mind: 1) the use of some sort of hybrid packaging to achieve greater packing density and/or 2) the ultimate use (when they become available) of memory devices with greater bit capacities.

Sperry Gyroscope has developed a hybrid packaging approach which uses 4-inch by 4-inch ceramic hybrid modules. Each module consists of four 2-inch x 2-inch "quads". Each quad can accommodate a 6 x 6 array of integrated circuits provided their average chip size does not exceed approximately 160 mils x 160 mils. Calculations have been made based upon this packaging approach for the 256-bit memory devices and also for future memory capacities of 1024 bits (256 x 4) and 4096 bits (1024 x 4). The results of these calculations for a 32K x 36 memory system are shown in table 10.

Power consumption and access time assumptions had to be made in view of the theoretical nature of the 1024-bit and 4096-bit devices and the incomplete information concerning the 256-bit memory chips. The assumptions for access time were that CMOS/SOS decode and buffer circuits on the memory chips would permit chip access times in the 200 to 250 nanosecond range, thereby allowing system access times of 500 nanoseconds, with the 256-bit devices somewhat faster. The power consumption figures were assumed as follows:

MEMORY CHIP CAPACITY	READ ONLY OPERATING POWER (mW)	STANDBY POWER (mW)
256	200	10
1024	400	15
4096	800	20

Table 10  
32K x 36 MNOS EAROM SYSTEM CHARACTERISTIC

	MEMORY CHIP CAPACITY		
	<u>256-BIT</u>	<u>1024-BIT</u>	<u>4096-BIT</u>
Read access time (ns)	450	500	500
Power (at 2 MHz, W)	50	23	14
Volume (cu. ft.)	0.35	0.1	0.06
Weight (lbs)	13	4	3
Chip count	5200	1400	425

The power totals in the table are primarily derived from the foregoing values for the memory chips. The control circuits have a very minor impact upon the numbers. No comparison of the power figures with the numbers specified in subsection 3C is possible because the latter pertain only to the control circuits, the memory chip power dissipation being an unknown.

Although over-all weight and volume are not specified in the SOW, one can calculate them very easily from the size, weight, and spacing of the individual boards. The results are approximately 4.25 pounds and 0.12 cubic feet. Note that these numbers are very close to the values in the center column of table 10. These numbers are for a memory chip with four times the capacity of the RCA 256-bit chip and for a hybrid packaging approach which provides denser packaging than the SMARC approach. Certainly it is very attractive to consider a hybrid packaging approach for a memory with 1400 integrated circuits and almost imperative for one with 5200.

## Section 4

### SUBSYSTEM PRODUCIBILITY

#### A. INTRODUCTION

There are two categories to consider in regard to the producibility and reliability of the three chip types proposed for this contract. The first is the conventional design which involves no radiation hardening in the processing and the second is the hardened design involving the Aubuchon process, aluminum ion implantation of n-channel transistors and diode clamping. The other design factors that relate to radiation resistance do not affect producibility or reliability in any way. Those other factors include the use of 2-input gates only and the tailoring of  $\alpha (W_p/W_n)$  for switching voltage alteration. The  $\alpha$  design modification does not increase chip area because p-channel width increases are balanced by n-channel width decreases.

#### B. PRODUCIBILITY

The producibility of standard CMOS/SOS circuits has been well established by the production history at Inselek. They have delivered 100,000 wafers containing SOS circuits. All of their production uses SOS technology and they are acknowledged to be leaders in that technology.

The particular chip designs generated on this contract are definitely within the state-of-the-art at Inselek at this time. The chip dimensions are not large except, perhaps, the Type A chip at 145 mils x 145 mils. However, Inselek already has larger chips in production such as the INS 4201, Cross Point Switch, which has chip dimensions of 145 mils x 170 mils.

There are no unusual aspects to the chip designs that would adversely affect their producibility. The chips could be produced today, if necessary, and Inselek has estimated the development and production costs for all three chips.

The producibility of the hardened versions of these chips is clearly not as readily demonstrable. However, the hardening approach taken uses most of the steps employed in the standard proven commercial process and consequently presents minimum risk. The main elements of the process and an estimate of their effect upon producibility and yield are presented below.

As indicated in subsection 2E, the hardening process is based on Aubuchon's procedures for p-channel transistors under negative potential, aluminum implantation only on n-channel transistors under positive potential, and the prevention of opposite polarities on either channel type by connecting their gates, when necessary, to appropriately directed diodes. This approach combines the successful elements of two approaches. The hardening does entail increased costs, resulting from the increase in circuit area and design complications caused by the clamping gate diodes. Other contributing factors are the larger number of process steps due to masking and aluminum implantation and the consequent decrease in yield.

The process steps are outlined in table 11. The steps important to hardening are marked with an asterisk and are described below.

Table 11  
PROCESS STEPS FOR HARD CMOS/SOS

1. n-epitaxy
2. p-implantation
3. n, p diffusion
4. Silicon etch
- 5.\* Oxide preclean
- 6.\* Oxidation
7. Mask for contact etch
8. Etch contact holes
- 9.\* Mask for implant

Table 11 (Cont'd)  
PROCESS STEPS FOR HARD CMOS/SOS

- 10.\* Aluminum implant
- 11.\* Anneal
12. Metallization preclean
- 13.\* Aluminum evaporation
14. Metallization mask
15. Etch aluminum
- 16.\* Sinter aluminum
17. Dicing and mounting
18. Wire bond
19. Pre-seal test
20. Seal
21. Final Test

### 1. CLEANING

This sequence of steps consists of the removal of the protective oxide, heating in concentrated sulfuric acid, etching in peroxide and ammonia solution, and then in peroxide and hydrochloric acid solution, rinsing in de-ionized water and then drying in absolute alcohol and in freon. Oxidation must follow immediately afterwards.

### 2. OXIDATION

The slice is heated to  $1020^{\circ}\text{C}$  while ultra-high-purity argon flows through the reactor. When that temperature has been reached a mixture of 2% hydrochloric acid in ultra-high-purity oxygen replaces the argon, and the temperature and gas mixture are maintained for two hours.

At the end of this period, the  $\text{HCl}-\text{O}_2$  mixture is replaced by ultra-high-purity argon and the slice is cooled.

### 3. ALUMINUM IMPLANTATION

Implantation is done at 10-20 keV using an ion current near  $5\mu\text{a}$ . The implantation of ten slices takes about 2 hours to reach  $10^{14}$  atoms per square centimeter aluminum concentration.

#### 4. ANNEALING

After the photoresist is removed by hot sulfuric acid, followed by cleaning, the slice is annealed. This is accomplished by heating at 450°C for 30 minutes in dry nitrogen.

#### 5. ALUMINUM EVAPORATION

The slices are stacked in the planetary fixture within the evaporator which ensures good aluminum coverage of the steps existing at the edge of the islands of silicon defined on the sapphire substrate. The source is a carbon crucible heated resistively and loaded with "five nines" (99.999) aluminum. The evaporation is maintained at a rate of 1500 Å per minute until the full 10,000 Å of aluminum have been deposited.

#### 6. SINTERING

Sintering is accomplished by placing the clean slice for 12 minutes in a furnace maintained at 512.5°C in a flow of ultra-high-purity argon.

Estimates of the cost of the hardening process can be made as follows: The estimates are considered conservative.

Cost increases arise from three sources. The first is the increased cost of slice processing due to additional procedures such as masking, implantation, and annealing and also the greater care needed in the oxidation and evaporation steps. If a weight of unity is given to each high-temperature and masking step, the commercial CMOS/SOS process has a cost index of 14. The implantation procedures, itself, adds three more such steps and thus an added weight of 3. In addition, the increased difficulty of oxidation and evaporation can be estimated as an increase in their weights of 0.5 each for a total accumulated increase from 14 to 18. Thus the increased cost of slice processing is approximately 4/14 (roughly 30 percent). The second source of cost increase is the need to add area for diode clamping. An estimated 10-percent increase in such area will also increase the cost of each chip by the same amount. However, not all circuits would require this much increase in area. The value of 10 percent is a general estimate for average cases rather than a specific value calculated for the particular chip designs generated on this program.

The third and final source of cost increase over current production figures is due to a decrease in yield. Yield is inversely proportional to the number of masking steps and also to the chip area. It is estimated that each might contribute 10 percent to yield loss. Thus, the increase in manufacturing cost may be as high as 60 percent.

In addition, there are nonrecurring expenses associated with processing hardened CMOS/SOS. First, the purchase and installation of new equipment is necessary, most notably a non-radiative evaporator for aluminum deposition and an aluminum implanter. In addition there are the development costs of instituting new process variants for cleaning, oxidation, implantation, and evaporation. Included in the latter should be the cost effects of a learning curve as personnel gain the necessary experience to run the process smoothly. The incremental running cost of 60 percent given above assumes that the hardening process has been taken beyond the learning curve to production status.

### C. RELIABILITY

The reliability of the standard CMOS/SOS process at Inselek has been fairly well established by its production and field experience, although there is not a wealth of reliability data.

Table 12 shows reliability data taken for the Inselek INS4013S, a dual D-type flip-flop. One hundred devices were tested for 5000 hours at 125°C in an operating life test and only two failures were seen. This corresponds to an MTBF at 25°C of 3,840,000 hours.

In the absence of any data, it is hazardous to predict the effect of hardening process modifications on reliability. However, a rough and probably pessimistic estimate can be obtained based upon the expectation that reliability is inversely proportional to the number of high-temperature and masking steps in the processing. From numbers derived at the beginning of the previous subsection the decrease in reliability due to the increase in the number of steps should not exceed 30 percent.

Table 12  
CMOS/SOS RELIABILITY DATA

**Product Tested:** 1NS4013S - (Dual D-Type Flip-Flop)  
**Testing Started:** October 1, 1973  
**Parameters Monitored:** Functionality & Quiescent Power at 10V  
**Initial Quiescent Power Limit:** 20 $\mu$ W at 10V  
**Failure Definition:** Inoper. - Function Failure or Quiescent Power  
greater than 500 $\mu$ W at 10V

Test: Operating Life - 125°C MIL STD. 883, Method 1 1005, Cond. D

<u>Total Hrs.</u>	<u>Inoper.</u>	<u>125°C</u>	<u>55°C</u>	<u>25°C</u>
	Fail.	$\lambda$ MTBF	$\lambda$ MTBF	$\lambda$ MTBF
449,000	2	0.6% 166,000 hrs.	0.09% 1,110,000 hrs.	0.026% 3,840,000 hrs.

Test: Storage Life - 150°C, MIL STD. 883, Method 1008, Cond. C.

<u>Total Hrs.</u>	<u>Inoper.</u>	<u>125°C</u>	<u>55°C</u>	<u>25°C</u>
	Fail.	$\lambda$ MTBF	$\lambda$ MTBF	$\lambda$ MTBF
138,000	0	0.7% 143,000 hrs.	0.06% 1,670,000 hrs.	0.02% 5,000,000 hrs.

NOTES:  $\lambda$  = Demonstrated Failure rate (%/1000 hr.) at 60% confidence

MTBF = Mean time between failures based on  $\lambda$

$\lambda$  & MTBF at 55°C and 25°C are based on acceleration factors obtained from Report AD614103, Clearing House for Federal Scientific and Technical Information and Correspond to an Activation Energy of approx. 0.3 eV.

## Section 5

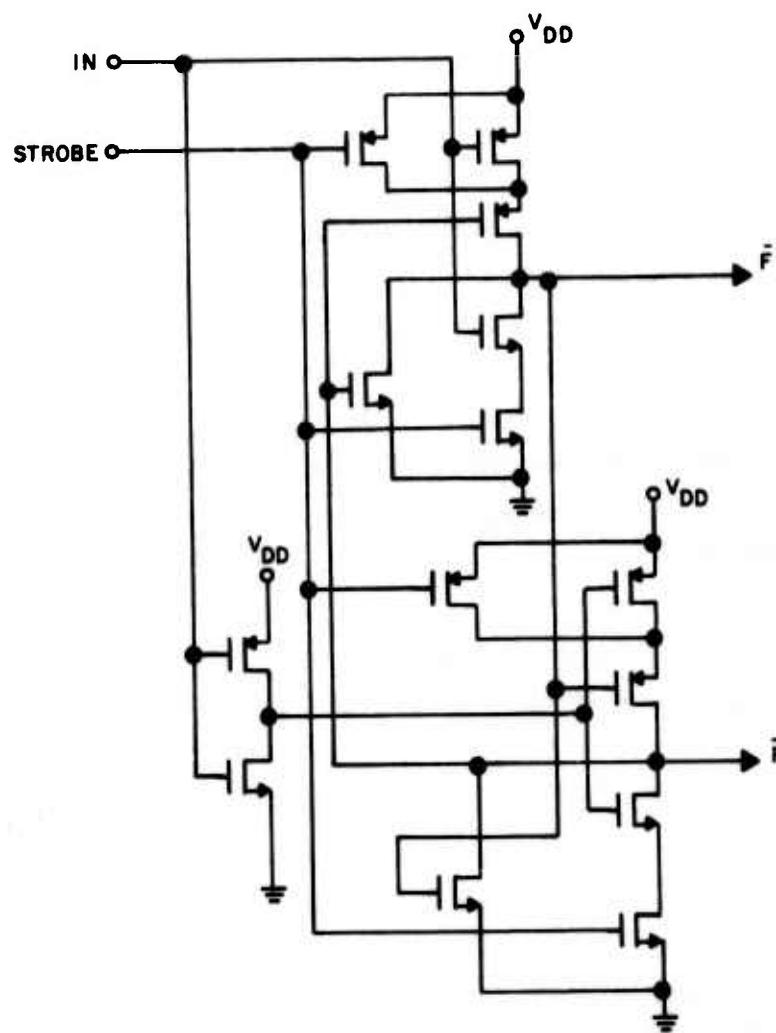
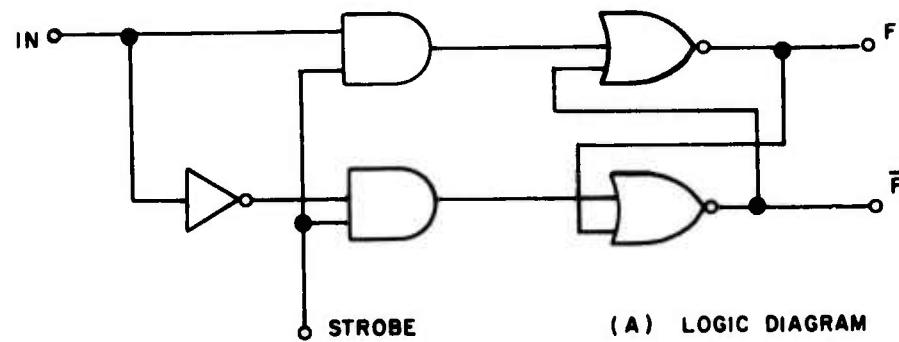
### SUMMARY AND CONCLUSIONS

#### A. FUTURE CONSIDERATIONS

In view of the fact that the contract called for design only and no fabrication, it is interesting to speculate on design variations which might lend themselves better to other system interface requirements or other memory chip or system capacities. Considering the Type A driver first, perhaps the most obvious possible variation is in the number of driver circuits on the chip. The use of 10 drivers lends itself nicely to a memory chip with 64 words (six address lines). However, if one had a larger chip, e.g., 256 words (eight address lines), with everything else the same, one would need 12 driver circuits on the chip to achieve the same subsystem partitioning.

This exceeds a pin count of 24 and also requires a chip area that is rather large for the near-term future state-of-the-art. In such a situation one could choose to back off to an eight driver chip and satisfy address and chip select driving requirements on separate chips. Of course a larger number of driver chips would be required but their smaller size would improve yield and reduce chip cost. In the context of a smaller number of driver circuits on the chip is a consideration of features which might be added if chip area were available.

It may be advantageous in some subsystems to incorporate a latch into each driver circuit to allow data, addresses, etc. to be strobed in, thereby freeing the interface from holding those lines steady for the length of time required by the memory. A possible approach to such a latch scheme is depicted in figure 23, along with the schematic equivalent for the latch part of the circuit. The strobe input goes high to



(B) SCHEMATIC DIAGRAM

Figure 23. Input Latch for Multi-Function Driver

permit the input to set the latch and then goes low to lock out the effect of any further changes on the input line. The effect upon chip area is not significant because the added devices are of small geometry and for that same reason the effect upon propagation delay time is small - an estimated increase of less than 10 nanoseconds.

Insofar as the Type B buffer chip is concerned, the possible variations in design can take advantage of the fact that the pin count of the proposed design is only 20 and the chip size is only 100 mils x 100 mils. If larger capacity memory chips were available and/or the allowable wire-OR connection at the memory were greater than four, a reduction in the number of buffers needed would be possible. This could be achieved by having an individual buffer chip provide several outputs to take care of several bits of the memory word.

Figure 24 shows a possible variation in which four bits are accommodated with a common enable line and a pin count of 23, including  $V_{DD}$  and  $V_{SS}$ . Propagation delay is actually reduced relative to the proposed design because, effectively one has four 4-input gates in parallel rather than one 16-input gate, thereby eliminating two series stages on the chip. As an example of the utility of such a design, consider its use in conjunction with a four-times larger memory chip (256 x 4) and an allowable wire-OR of eight memory chip outputs. The same 8K words of one section of memory would then require only 32 rows of memory chips. The wire-OR of eight rows would leave four lines that would need to be accepted by the buffer. Thus, the buffer of figure 24 would be just right and only nine such chips would be needed for the full 36-bit word, as compared to the 72 one-bit wide chips needed in the existing program. The four-bit wide buffer is even usable on the present program. One would still need 72 chips, however, and they would be larger and thus more expensive.

Possible variations in the Type D chip are not especially related to the memory chip capacity of the given program but are more a function of what logic the memory subsystem must perform. Consequently, speculation about potential variations in the chip design cannot be as profitable. Suffice it to say that the proposed design, despite its versatility, cannot be considered universal or best for all possible future applications.

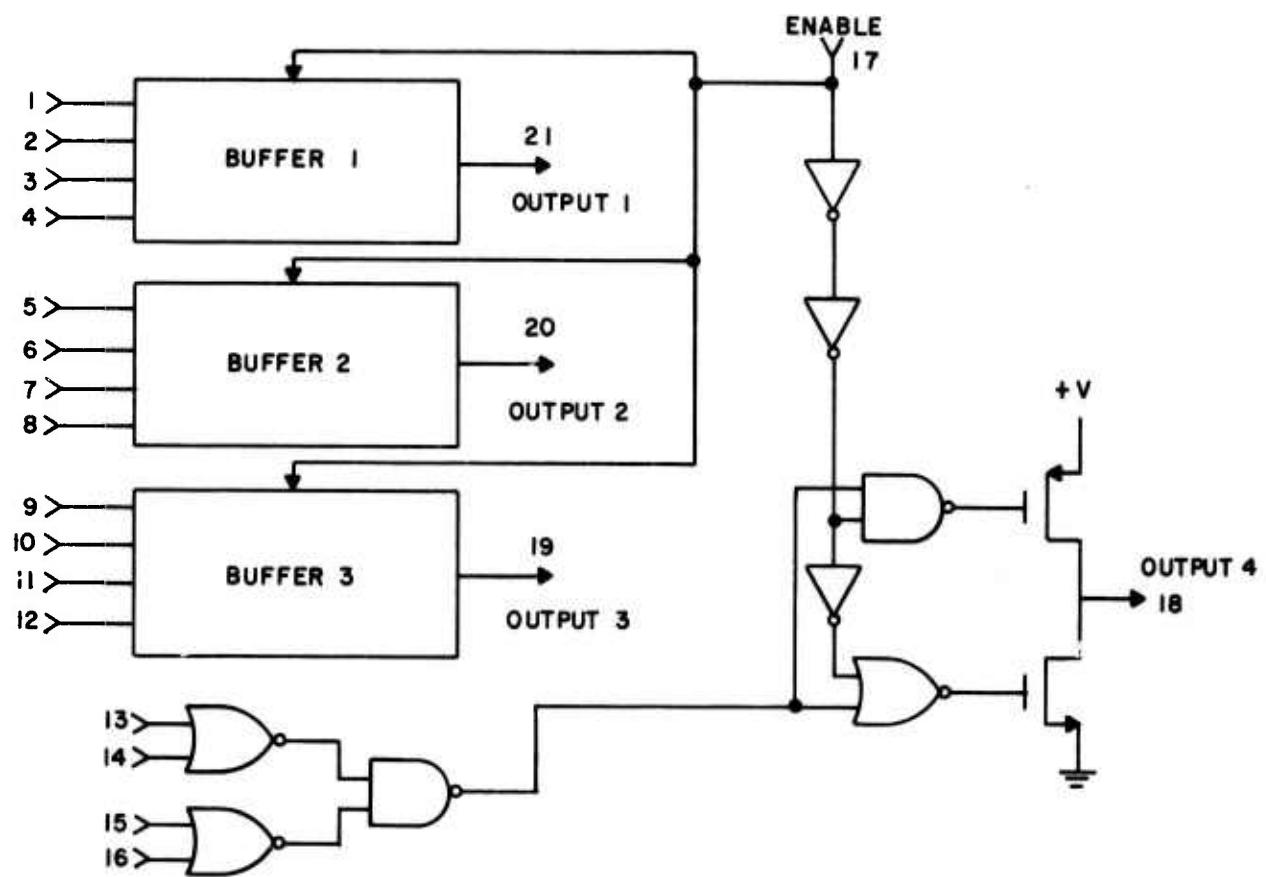


Figure 24. Four-Bit Data Output Buffer

## B. CONCLUSIONS

The foregoing variations have been considered to illustrate the fact that alternate designs are also practicable and may fit other systems better.

The designs proposed on this contract fit the system requirements very well and, in addition, have reasonable flexibility. If a standard electronic module with a greater degree of universality were desired, the designs could be modified toward that direction. Furthermore, approaches which use the same basic circuit layout mask, but employ varying metallization masks to end up with slightly different functional chips, are cost-effective and interesting.

The experience gained on this program will facilitate any alternate approaches which may be desired.

The designs which have been developed on this program demonstrate that it is quite feasible to achieve a memory subsystem using CMOS/SOS control circuits in conjunction with MNOS memory devices. Furthermore, it has been demonstrated that: 1) the control circuits can be a small number of chip types, at least for a static easy-to-use memory chip; 2) the quantity of control circuits can be a fairly small percentage of the quantity of memory chips; 3) practical steps may be taken to achieve varying degrees of radiation hardening; and 4) the circuits are producible with today's technology.